

LCFC Confidential


AILZA/B/C (ZX10)

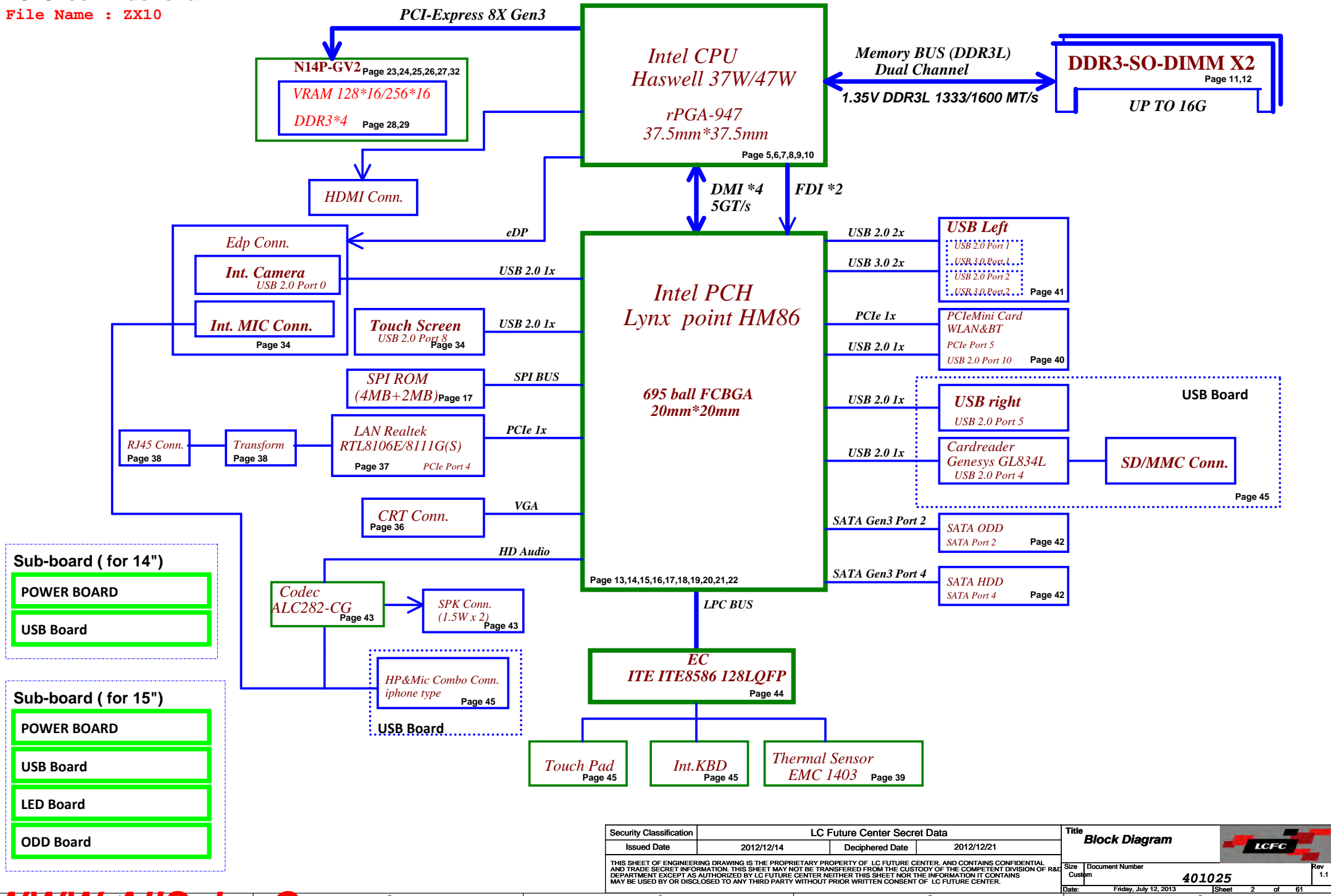
MB MA181 Schematics

Intel Haswell Processor with DDRIII L + Lynx Point HM86
nVIDIA N14P-GV2

2012-12-27

REV:1.1

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3V_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.675VS +CPU_CORE +VGA_CORE +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	X	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
EHCI1	XHCI 1	0	Camera
		1	USB Port (Left Side)
		2	USB Port (Left Side)
		3	
		4	Cardreader
		5	USB Port (Right Side)
		6	
EHCI2	2	7	
		8	TOUCH PANEL
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	

BOM Structure Table

BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	External GPU SKU ID part
UMA@	UMA SKU ID part
14@	For 2410 part
15@	For 2510 part
8106@	8106E LAN part
8111G@	8111G LAN Part
8111GS@	8111GS LAN Part
N14PGV2@	N14P GV2 stuff
GIGA@	GIGA LAN Part
Gastube@	Gastube Part
NOTIS@	No Touch screen part
GC6@	GPU GC6 function part
Tse	Touch screen part
@	Not stuff
ME@	Connector
XDP@	XDP part
37@	37W CPU part
47@	47W CPU part
H2@	Hynix 2Gb Vram part
M2@	Micron 2Gb Vram part
M4@	Micron 4Gb Vram part
S2@	Samsung 2Gb Vram part
S4@	Samsung 4Gb Vram part
M1GB@	Micron 1GB Vram BOM
M2GB@	Micron 2GB Vram BOM
S1GB@	samsung 1GB Vram BOM
S2GB@	samsung 2GB Vram BOM
H1GB@	hynix 1GB Vram BOM

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	PCH	TP Module	Charger	XDP
EC_SMB_CK1	IT8586E		V	V	X	X	X	X	X	V	X
EC_SMB_DA1	+3VALW	X	V	V	X	X	X	X	X	V	X
EC_SMB_CK2	IT8586E	V	X	V	X	X	V	V	X	X	X
EC_SMB_DA2	+3VS	+3VS_VGA		+3VS			+3VS	+3V_PCH		X	
PCH_SMBCLK	PCH	X	X	X	V	V	X	V	V	X	V
PCH_SMBDATA	+3V_PCH				+3VS	+3VS		+3V_PCH	+3VS		+3VS

PCIe PORT LIST

Port	Device
1	
2	
3	
4	LAN
5	WLAN
6	
7	
8	

	Fixed Signals				Muxed Signals		Fixed Signals				Muxed Signals		Fixed Signals			
HM86	USB3 1	USB3 2	NA	NA	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 6Gb/s 4 (1b)	SATA 6Gb/s 5 (1b)	SATA 3Gb/s 0	NA
					USB3 3 (01)	USB3 4 (01)							PCIE 1	PCIE 2 (0b)		NA
HM87 QM87	USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 6Gb/s 4	SATA 6Gb/s 5	SATA 6Gb/s 0	SATA 6Gb/s 1
					USB3 3	USB3 4							PCIE 1	PCIE 2	SATA 3Gb/s 2	SATA 3Gb/s 3

Soft Strap: (USB3P4_PCIE2_MODE)
 00: PCIe Lane 2 is statically assigned to PCIe Express (or GbE)
 01: PCIe Lane 2 is statically assigned to USB3 Port 4
 Soft Strap: (USB3P3_PCIE1_MODE)
 00: PCIe Lane 1 is statically assigned to PCIe Express (or GbE)
 01: PCIe Lane 1 is statically assigned to USB3 Port 3

Config	GPIO16,49
SATA4,SATA5	11
PCIE1,PCIE2	00

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

Device	Address	Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb	DDR DIMMA	0xA0
Charger	0001 0010 b	VGA	0x9E	DDR DIMMB	0xA2
		PCH	0x96	Wlan	Rsvd
				TP	0x2C for Synapsics 0x15 for ELAN vendor

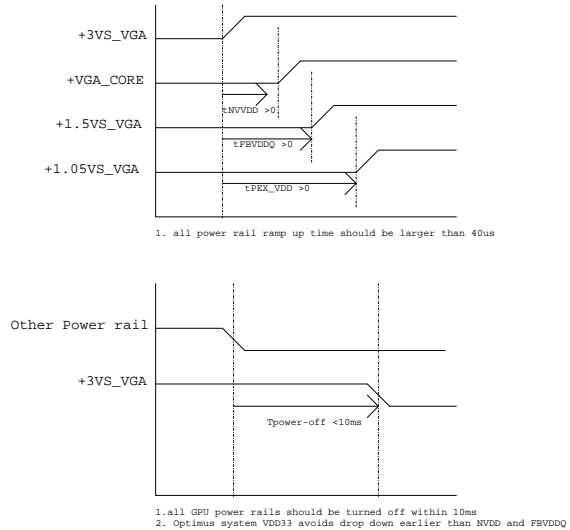
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VGA and GDDR3 Voltage Rails (N14P GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	IN	-	FB Clamp monitor
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5		N/A	
GPIO6	OUT	-	Active low FB Clamp toggle request
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



Performance Mode P0 TDP at Tj = 102 C* (DDR3)

	GPU (4)	Mem (1.5)	NVCLK /MCLK	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLL VDD (1.8V)		I/O and PLL VDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14P 64bit 1GB/2GB DDR3	25W	TBD	1000MHz	TBD	32	TBD	1.7	2.55	TBD	TBD	1.98	2.1	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

GPU	Device ID	SMB_ALT_ADDR (ROM_SO Bit 1)	setting	I2C Slave addrees ID
N14P-GV2	0x1292		0	0x9E (Default)
			1	0x9C

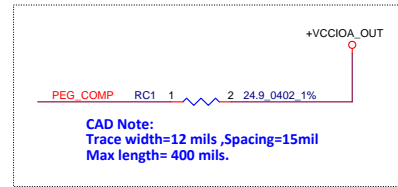
GPU	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GV2	TBD	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PD 15K	PD 4.99K	PU 45.3K

GPU		N14P_GV2		
FB Memory (DDR3)		ROM_SI		
Samsung 1GHz	K4W2G1646E-BC1A	0x7		
	128M x 16	PD 45.3K		
Micron 1GMHz	MT41J128M16JT-093G:K	0x5		
	128M x 16	PD 30.1K		
Hynix 1GMHz	H5TC2G63FPR-11C	0x4		
	128M x 16	PD 24.9K		
Samsung 900MHz	K4W4G1646B-HC11	0x3		
	256M x 16	PD 20K		
Micron 900MHz	MT41K256M16HA-107G:E	0x1		
	256M x 16	PD 10K		

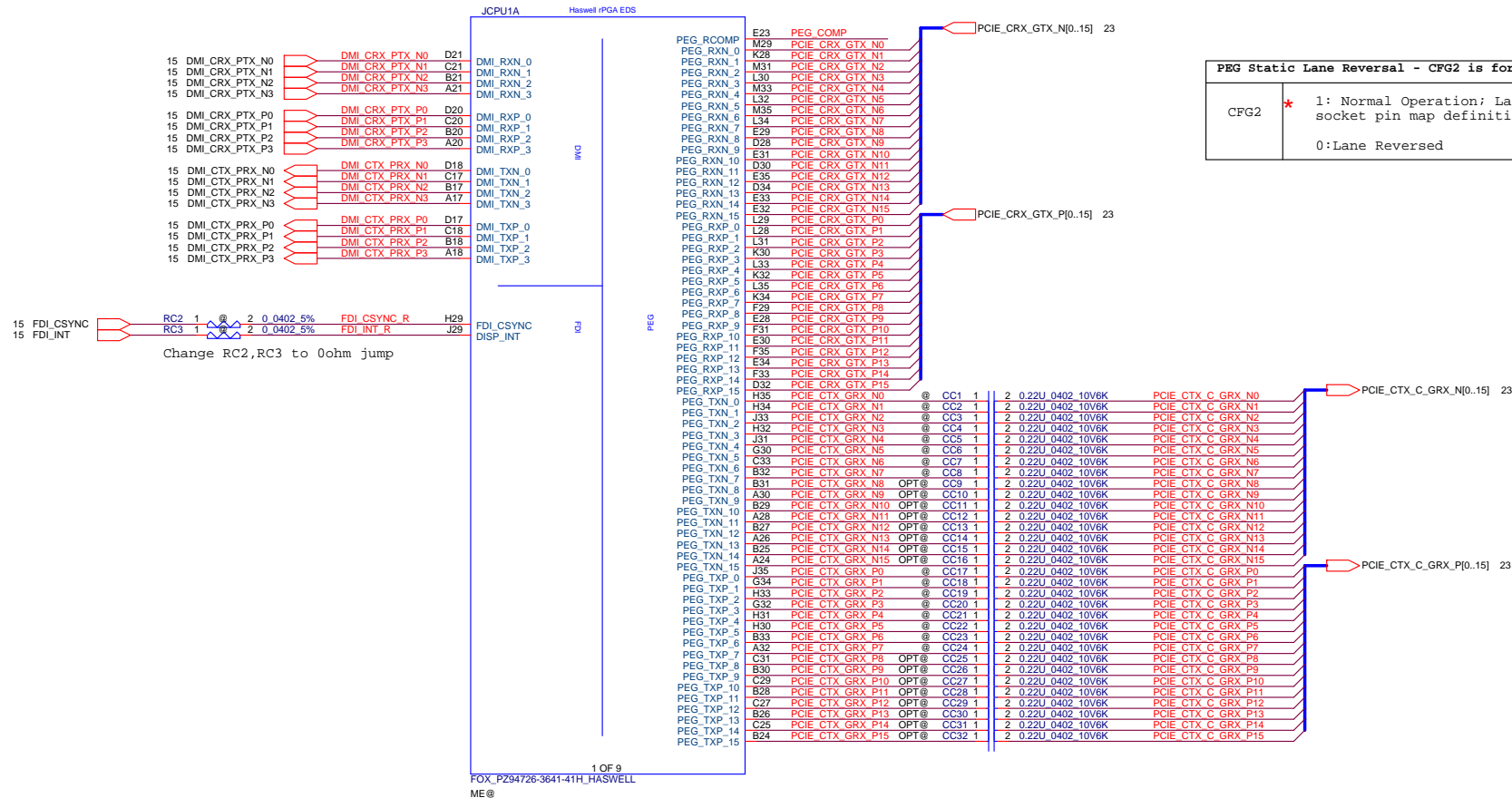
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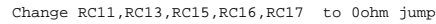
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PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>



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19 CPU_PLTRST# RC22 1 @ 2 0.0402_5% BUF_CPU_RST#

For ESD

1 2

CC35
220P_0402_50V7K

2

1 2

CC36
220P_0402_50V7K

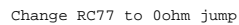
2



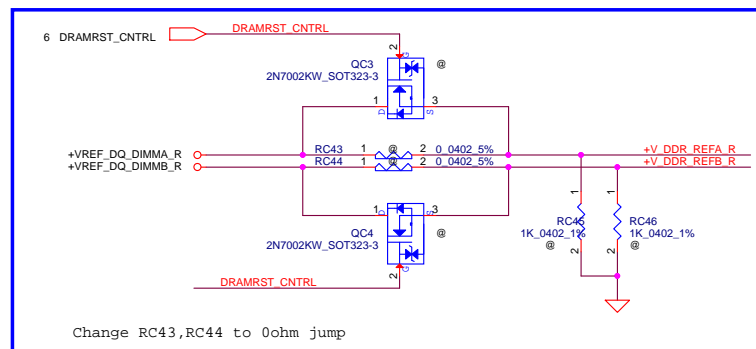
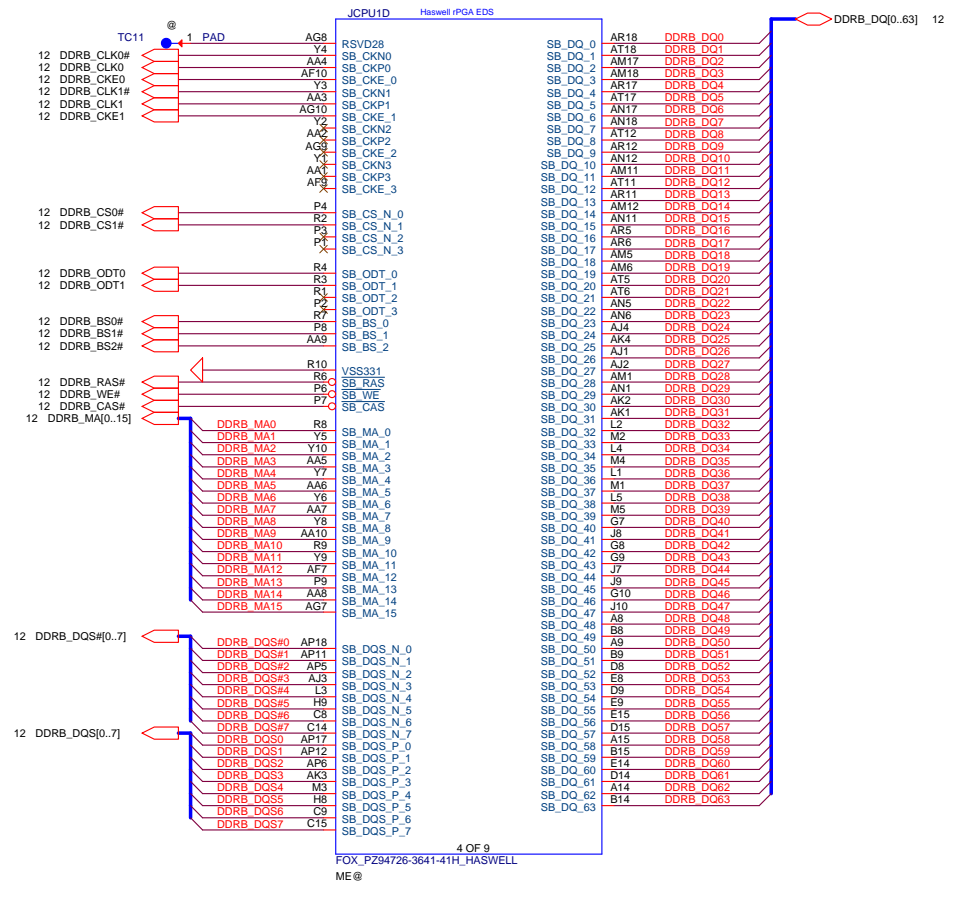
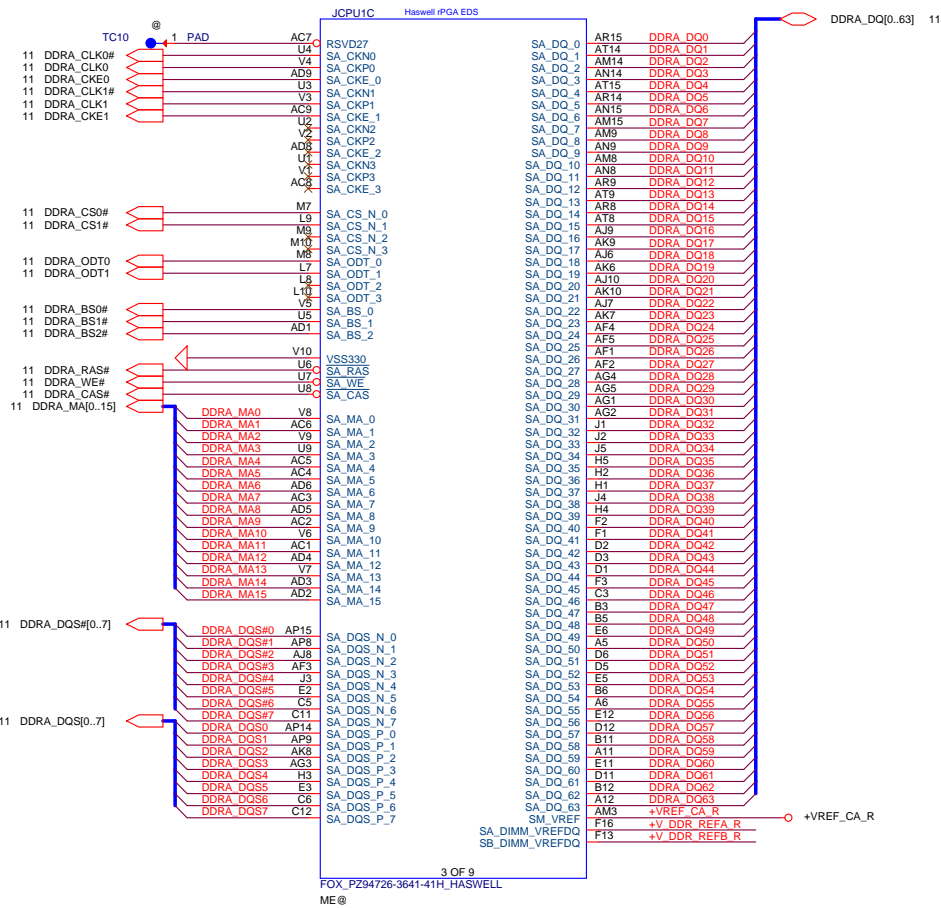
Timing diagram for the XDP module. The signals shown are:

- XDP_DBRESET# R**: RC14 2, 1 1K 0.402 1%
- XDP_TMS @**: RC18 2, 1 51 0.402 1%
- XDP_TDI R**: RC19 2, 1 51 0.402 1%
- XDP_PREQ# @**: RC20 2, 1 51 0.402 1%
- XDP_TDO R**: RC21 2, 1 51 0.402 1%
- XDP_TCLK**: RC23 2, 1 51 0.402 1%
- XDP_TRST#**: RC24 2, 1 51 0.402 1%

The diagram also shows power supply rails: +3VS and +1.05VS.

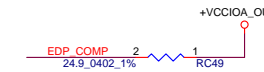
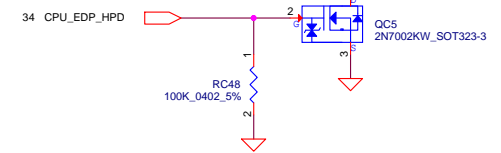
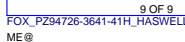
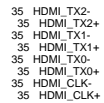


Title			
CPU (2/7) PM, XDP, CLK			
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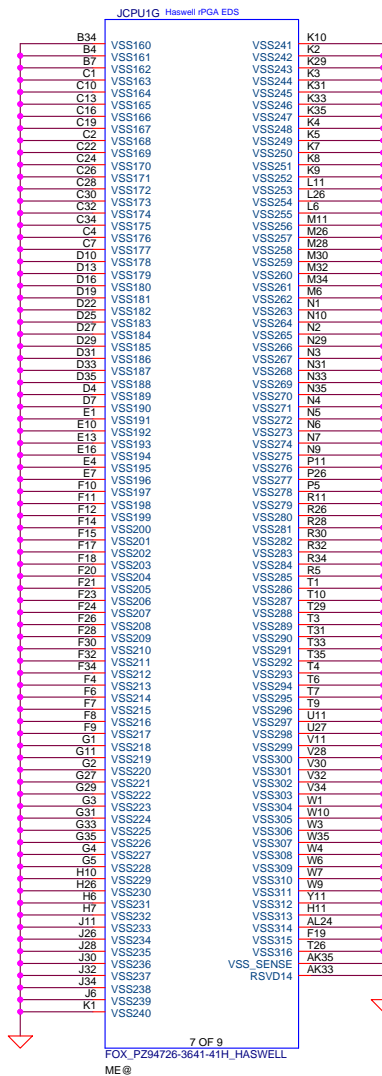
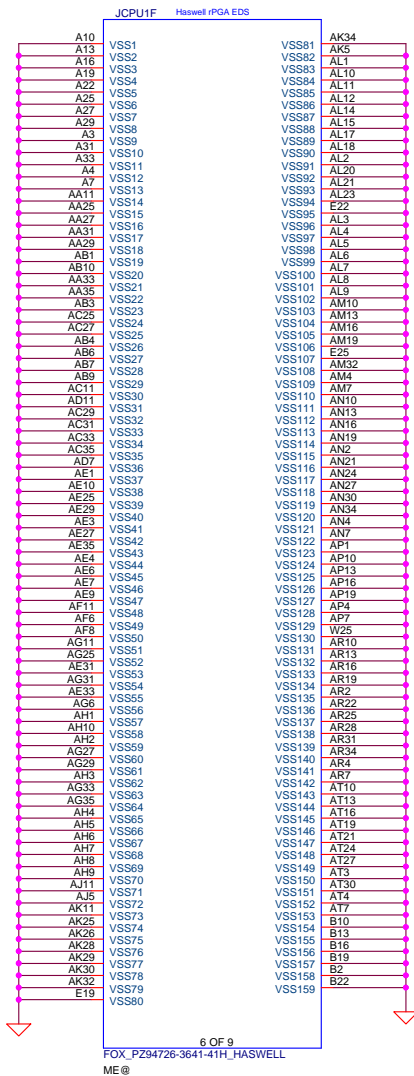
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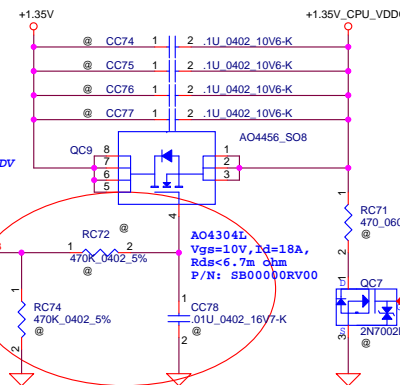
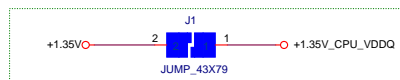
A schematic diagram showing a resistor labeled "RC53 1K_0402_1%" connected between a pin labeled "CFG2" and ground. The resistor is represented by a blue zigzag line with terminals labeled "1" and "2". Terminal "1" is connected to the "CFG2" pin, and terminal "2" is connected to a ground symbol (a triangle pointing down). A circled "@" symbol is placed near the resistor.

A schematic diagram showing a signal source labeled 'CFG7' connected to a 1k resistor. The resistor is labeled 'RC55 1K_0402_1%' and has terminals '1' and '2'. The other end of the resistor is connected to ground, represented by a triangle symbol.

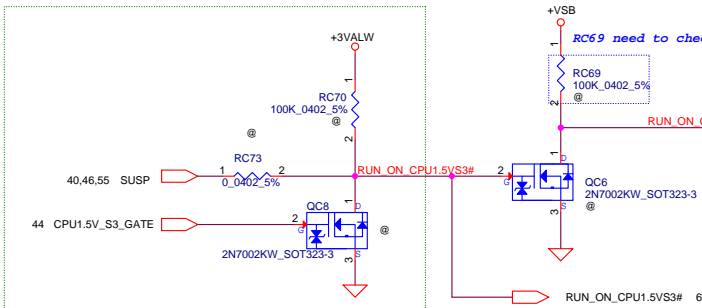
Need confirm with Intel if this reserved circuit can be deleted.



+1.35V_CPU_VDDQ



For Deep S3

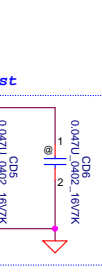
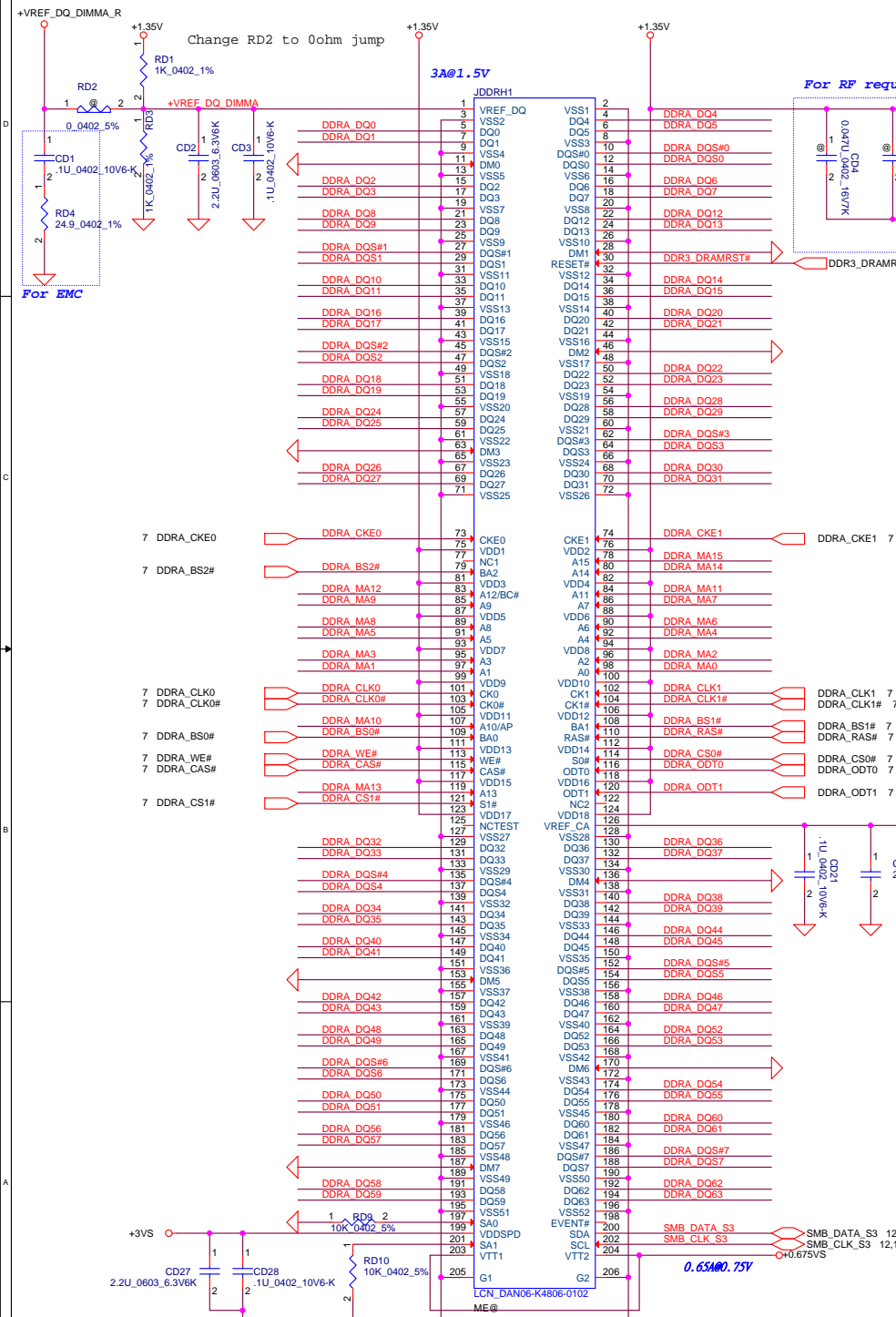


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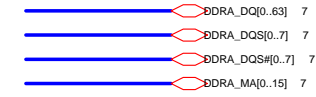
Title			
CPU (6/7) PWR			
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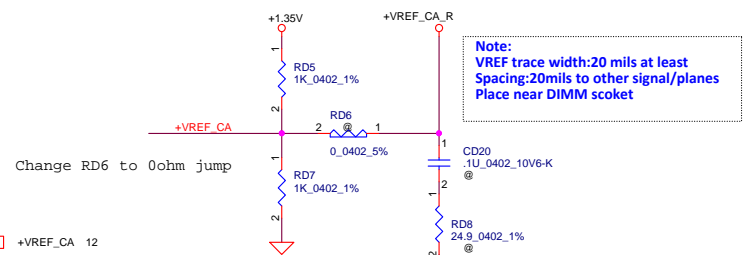
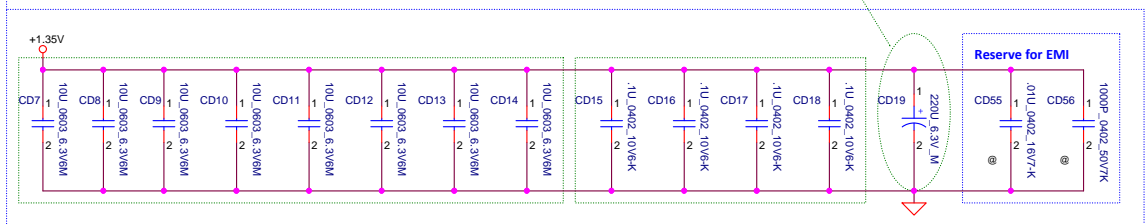
DDR3 SO-DIMM A



Layout Note:
Place near DIMM

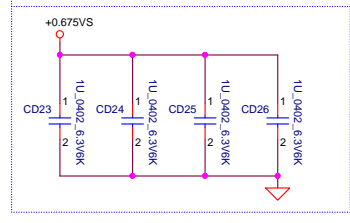


OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4



Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

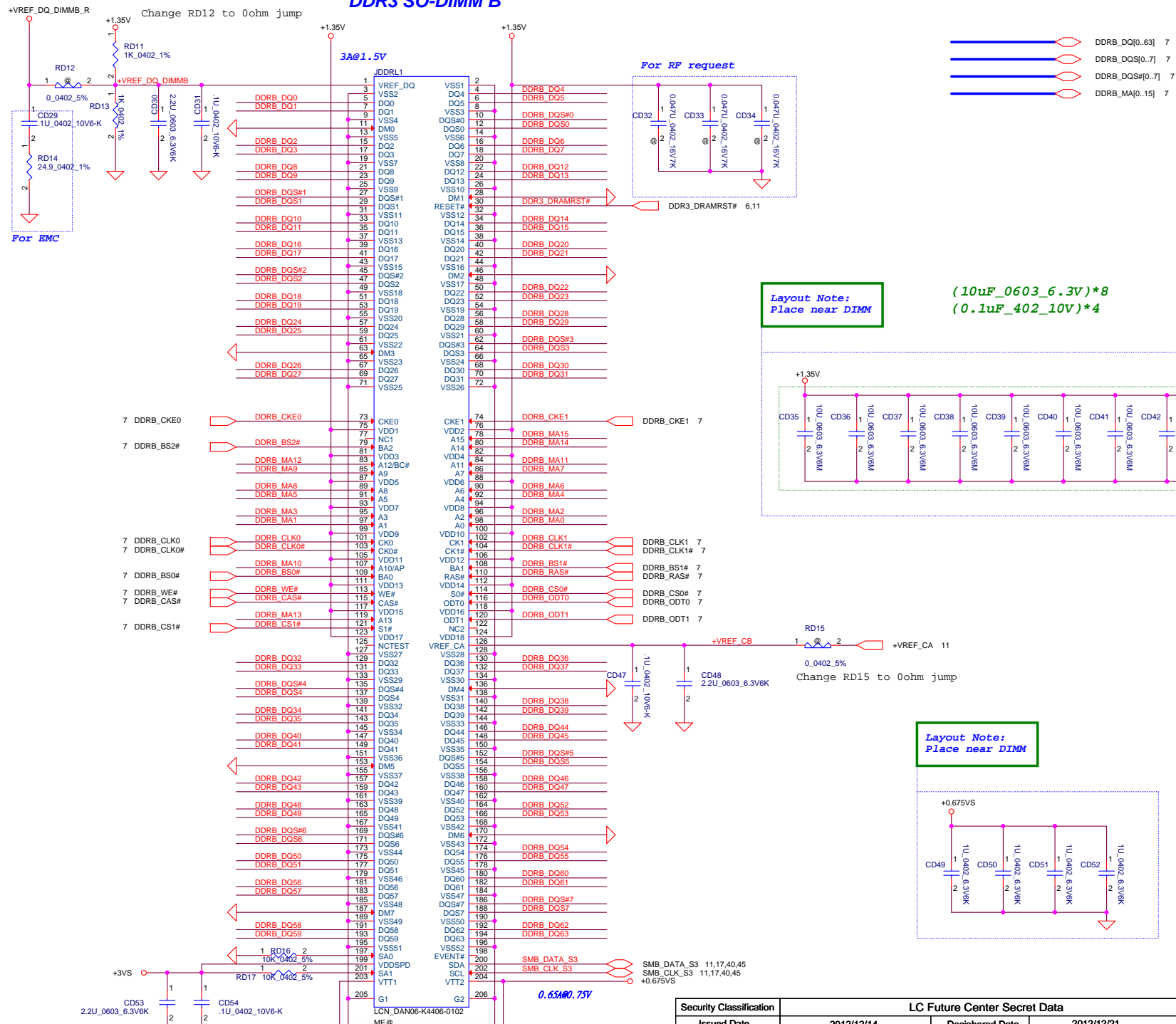






DDR_A_DM[0:7] connect to GND

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DDR3 SO-DIMM B



	DDR_B_DQ[0..63]	7
	DDR_B_DQS[0..7]	7
	DDR_B_DQS#[0..7]	7
	DDR_B_MA[0..15]	7

Layout Note:
Place near DIMM

$$(10\mu F_{0603_6.3V}) * 8$$

$$(0.1\mu F_{402_10V}) * 4$$

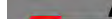
Layout Note:
Place near DIMM

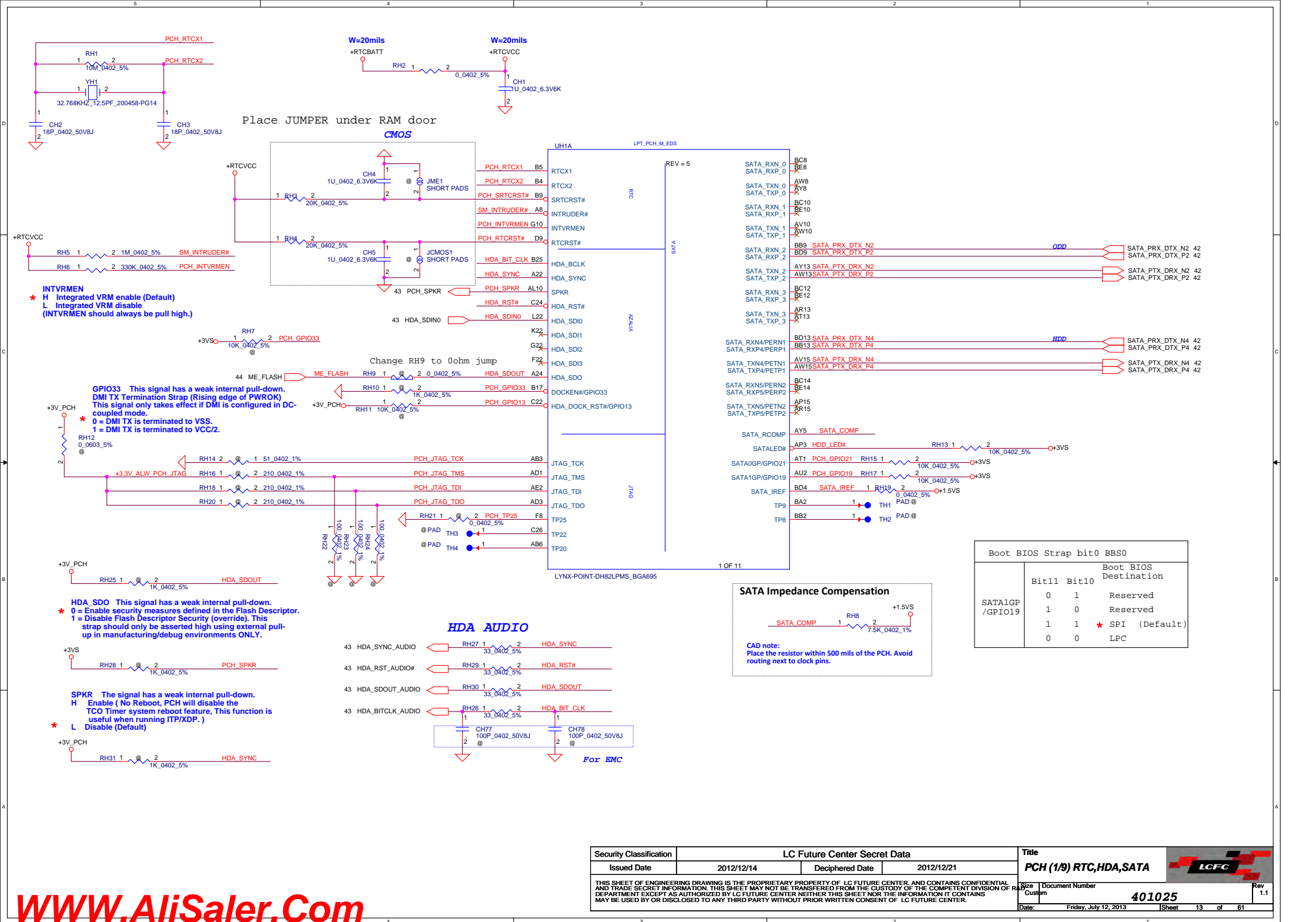
Layout Note:
Place near DIMM

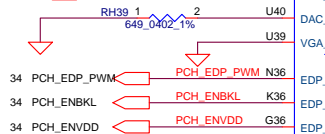
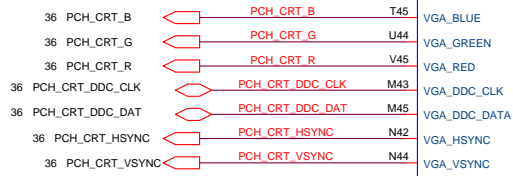
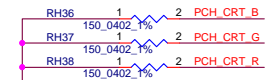
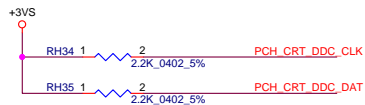
DDR_B_DM[0:7] connect to GND

The circuit diagram shows a 4-bit parallel adder implemented using two 74181 4-bit ALUs and one 74180 4-bit majority gate. The 74181 ICs are configured with their A inputs (pins 1, 2, 3, 4) connected to the 4-bit input A (A3, A2, A1, A0) and their B inputs (pins 5, 6, 7, 8) connected to the 4-bit input B (B3, B2, B1, B0). The carry-in input (pin 9) of the first 74181 is connected to a +0.675V source, and the carry-in input (pin 9) of the second 74181 is connected to the carry-out (pin 10) of the first 74181. The 74180 majority gate is configured with its four inputs (pins 1, 2, 3, 4) connected to the outputs of the two 74181s (pins 10, 11, 12, 13) and its carry-in input (pin 5) connected to the carry-in of the first 74181. The majority gate's output (pin 6) is connected to the carry-in of the second 74181. The 4-bit outputs of the adder (S3, S2, S1, S0) are taken from the outputs of the two 74181s (pins 14, 15, 16, 17).

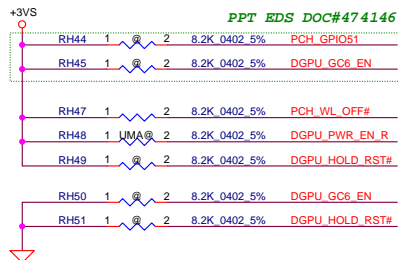
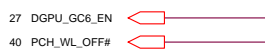
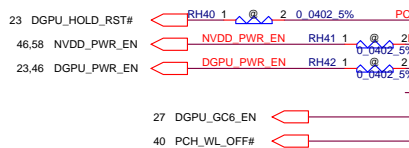
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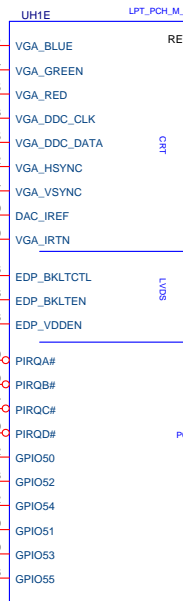
Change RH40, RH41, RH42 to 0ohm jump



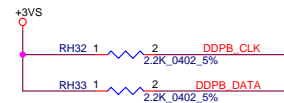
GPIO53 The signal has a weak internal pull-up.
H DMI is in DC-coupling mode (desktop, mobile or server/workstation).
L DMI is in AC-coupling mode (server/workstation only, not meant for desktop/mobile).



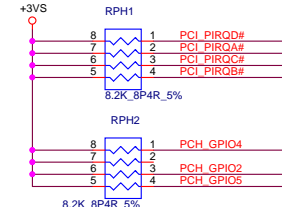
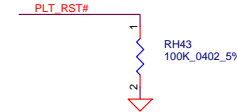
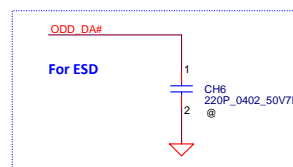
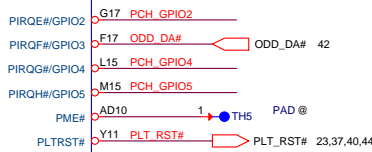
GPIO55 The signal has a weak internal pull-up.
H Disable 'Top-Block Swap' mode.
L Enable 'Top-Block Swap' mode.

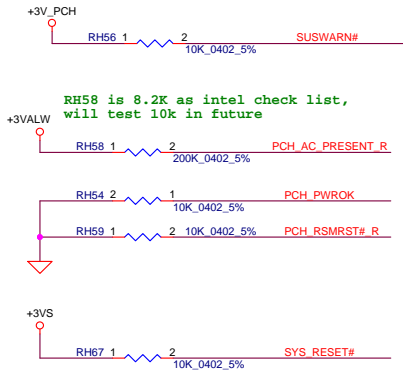
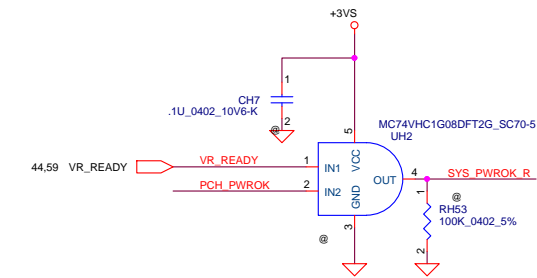


Boot BIOS Strap		
BBS_BIT1 (GPIO51)	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

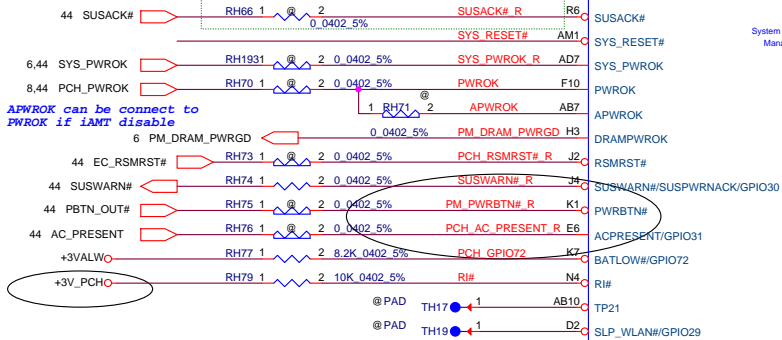


DDPB_CTRLCLK The signal has a weak internal pull-down.
H Port B is detected.
L Port B is not detected.



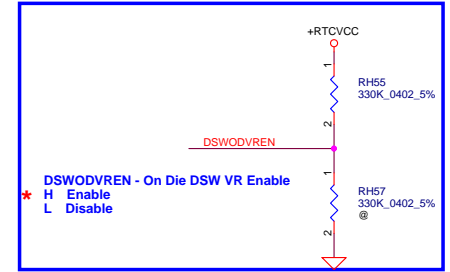
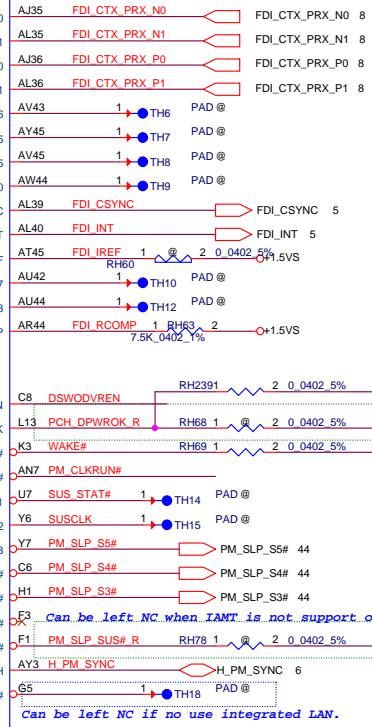
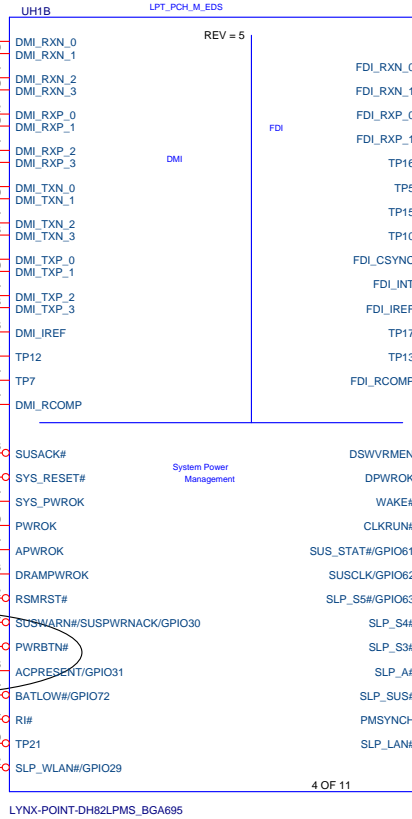
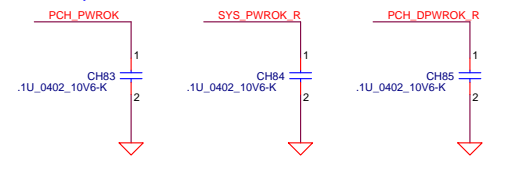


For Deep S3

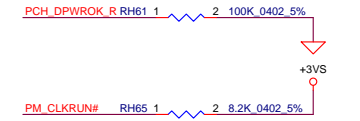


Change RH62, RH193, RH70, RH71, RH73, RH75, RH76, RH60 to 0ohm jump

AS EMC request

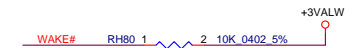


RH61 is 1% as check list request, CRB is 5%. follow CRB



For Deep S3
note need connect to GPIO27

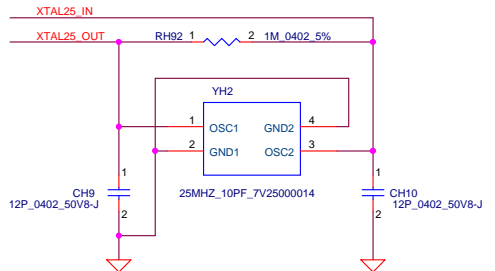
SUSCLK/GPIO62 - (Have weak internal pull-up)
PLL On-Die Voltage Regulator Enable
* H Enable
L Disable



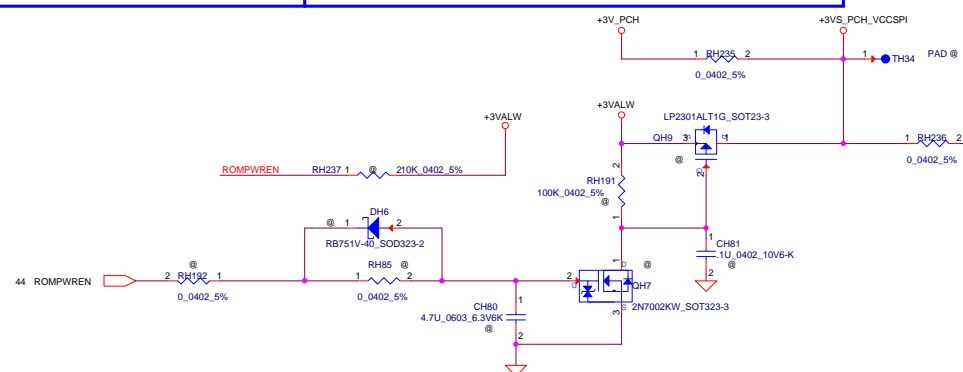
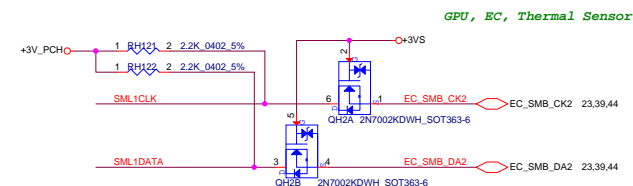
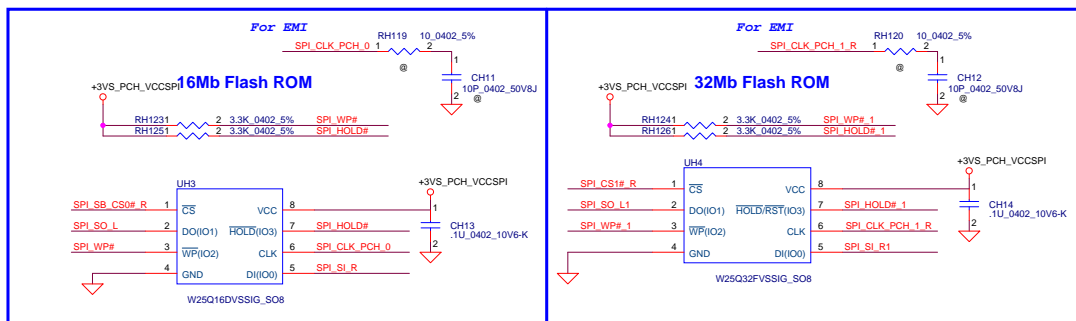
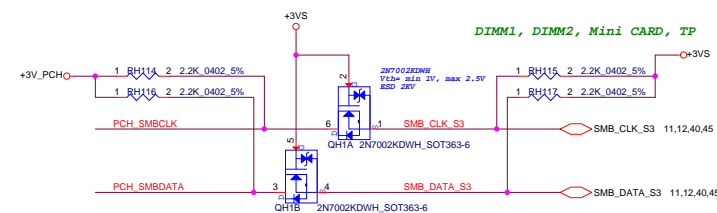
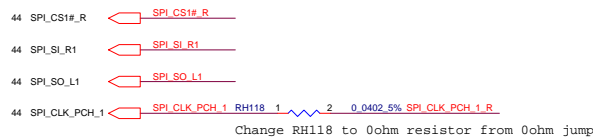
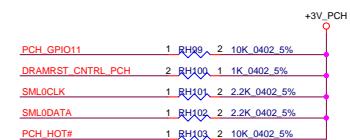
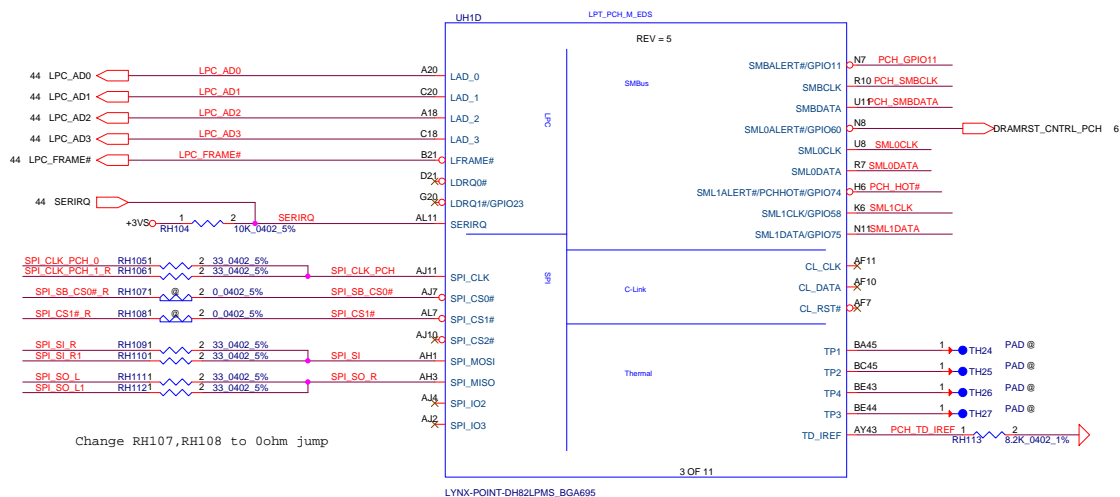
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Title			
PCH (3/9) DMI, FDI, PM			
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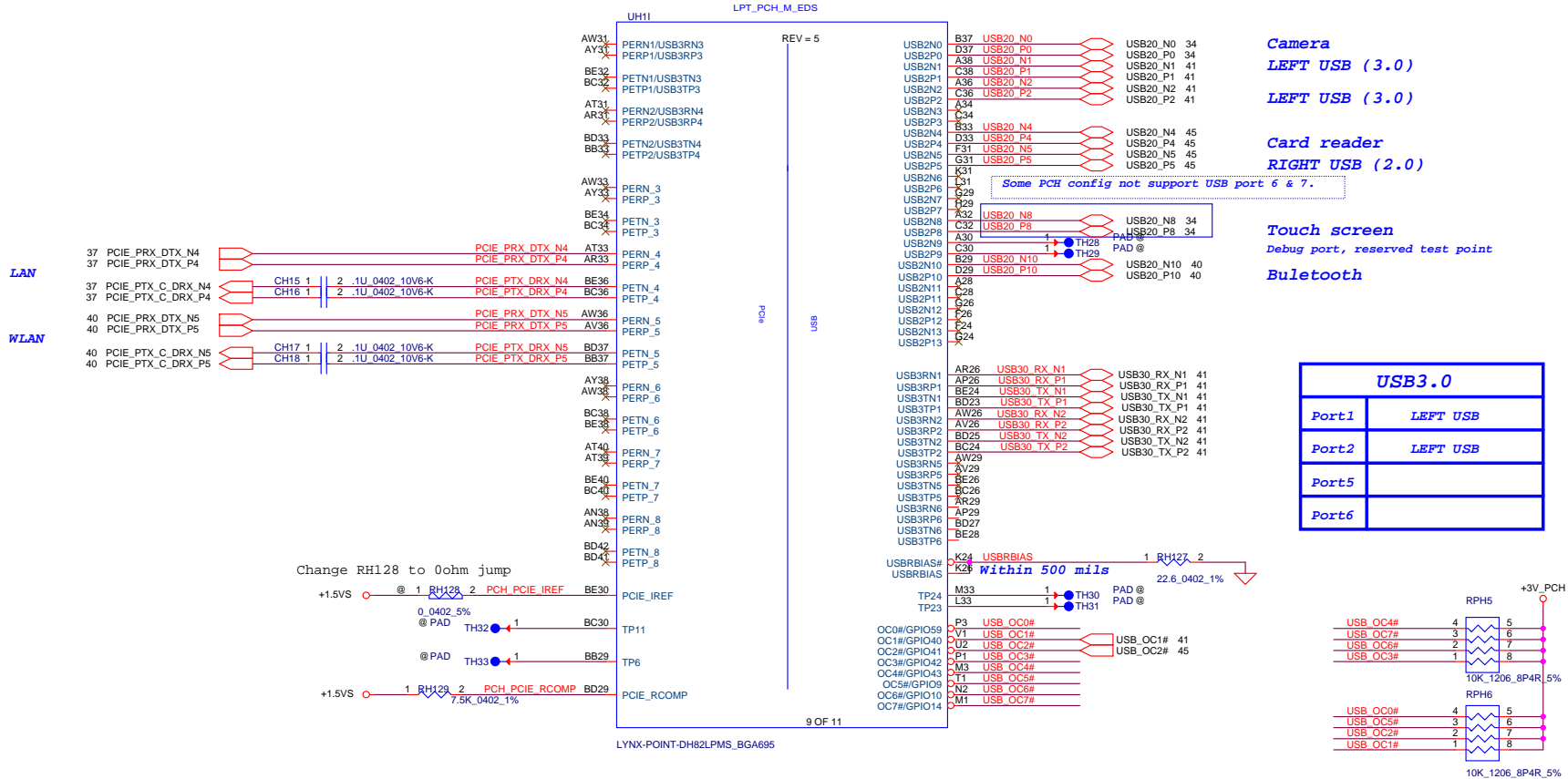


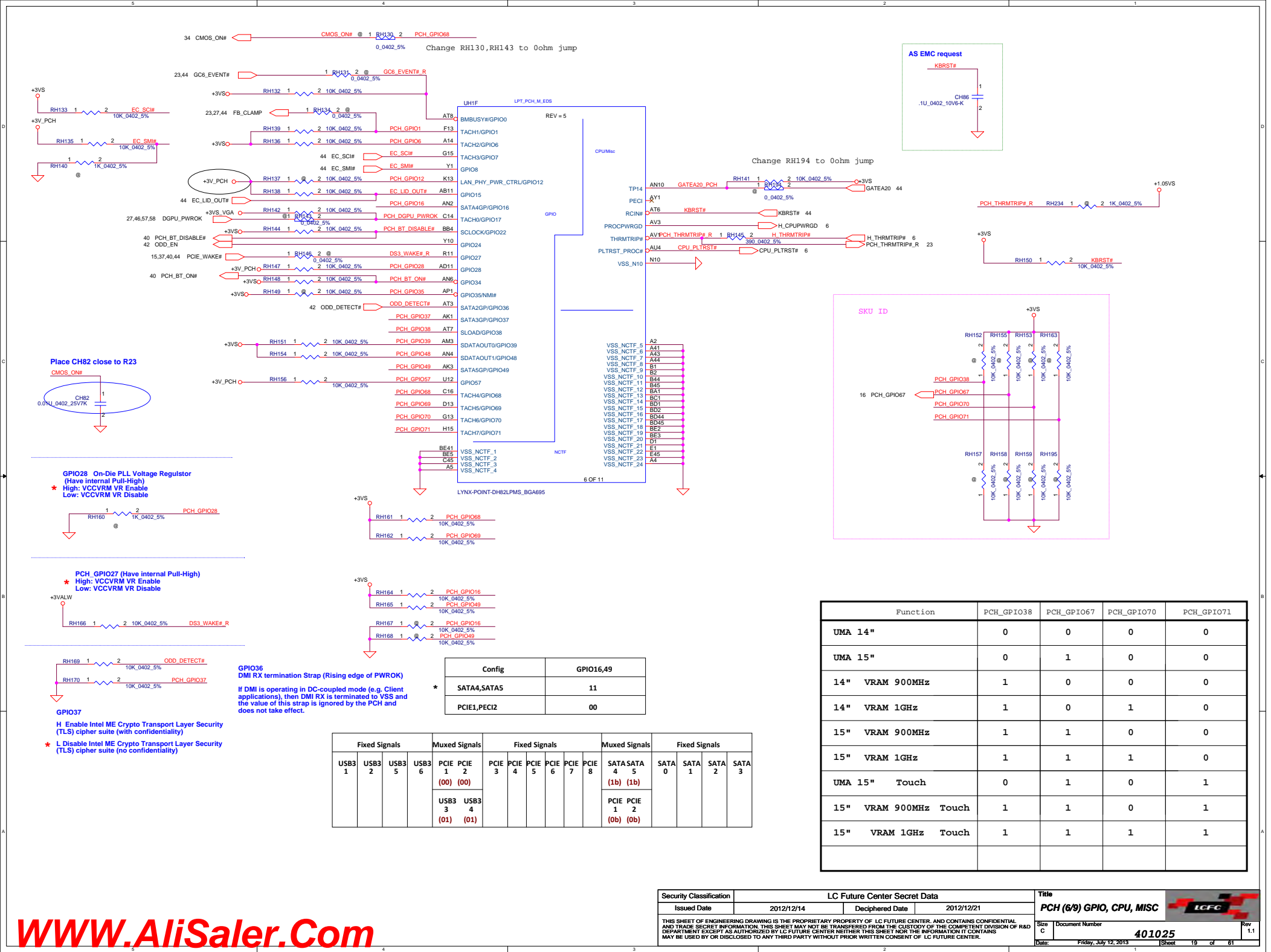


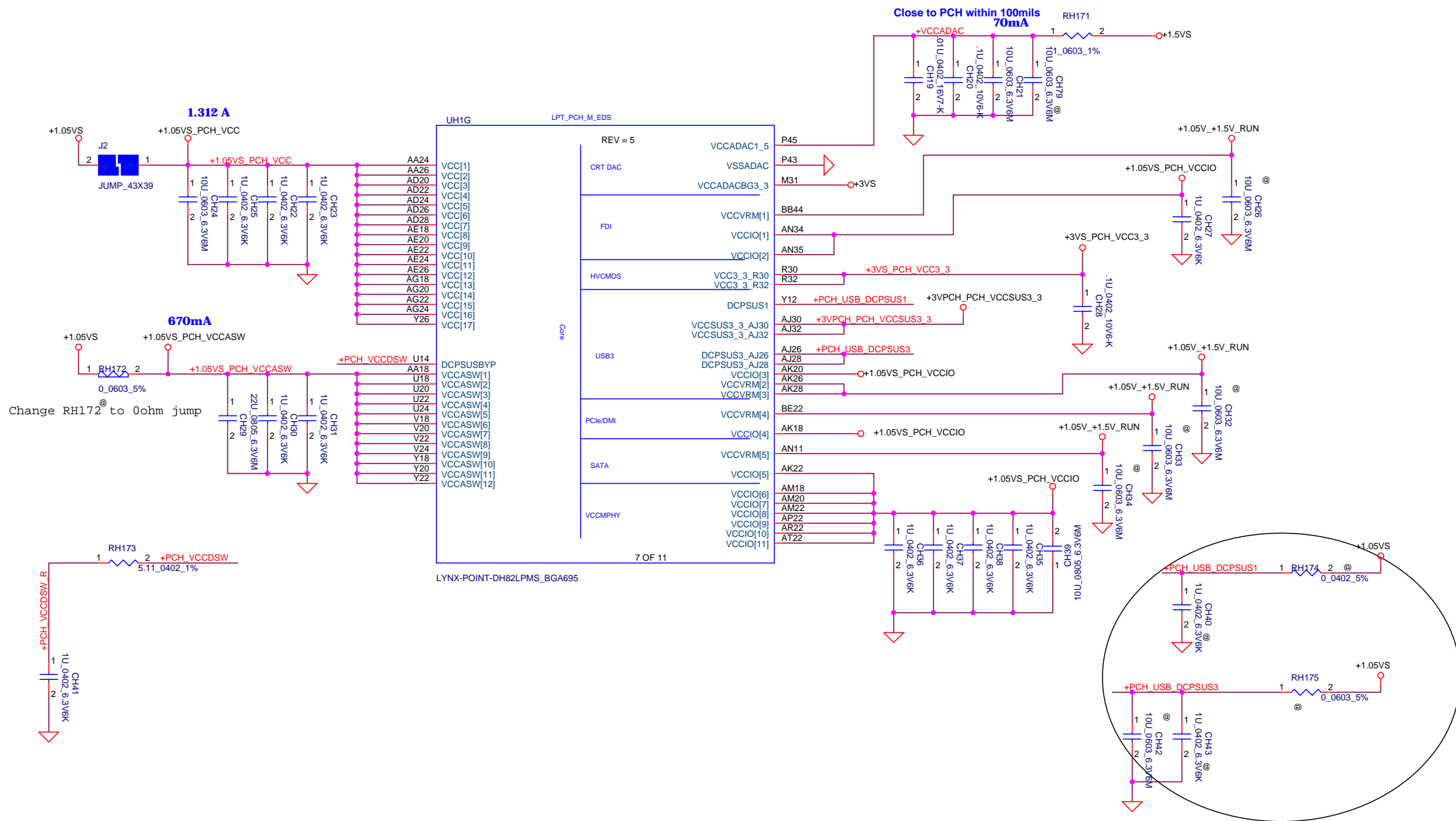
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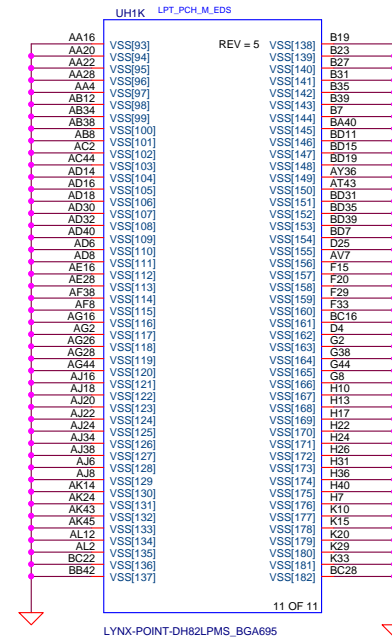
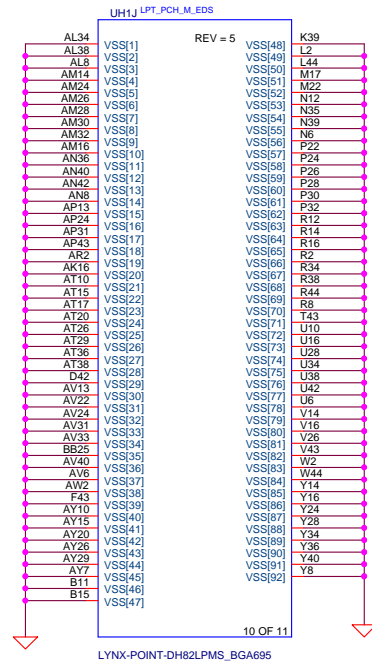





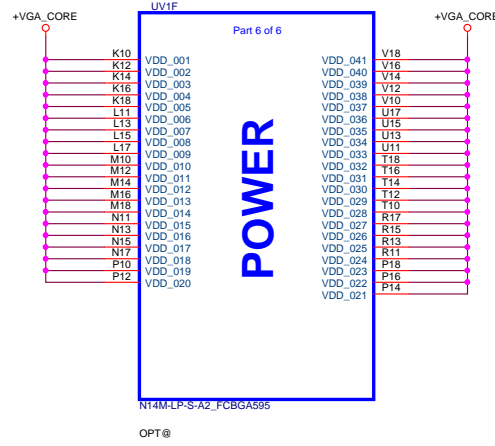
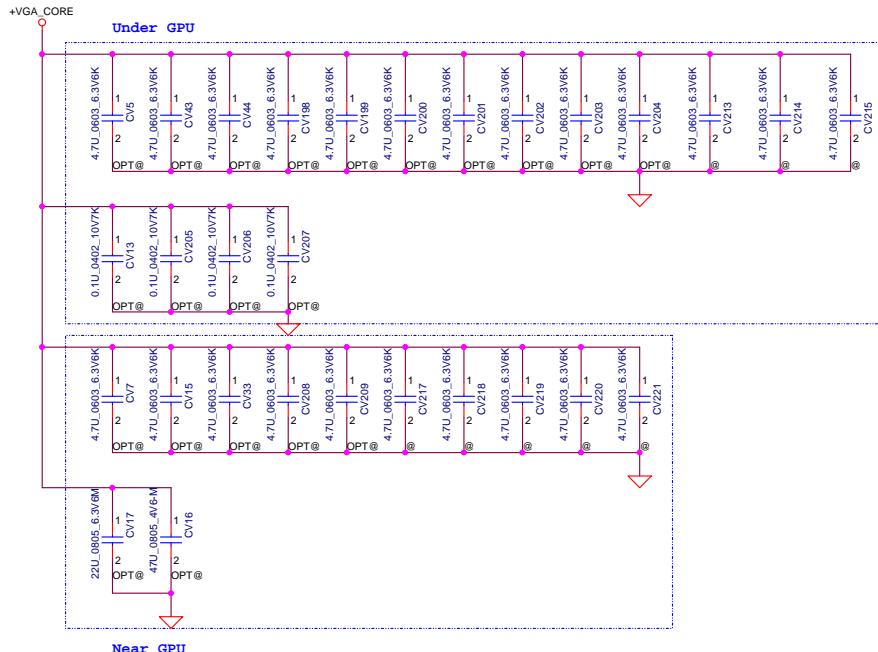
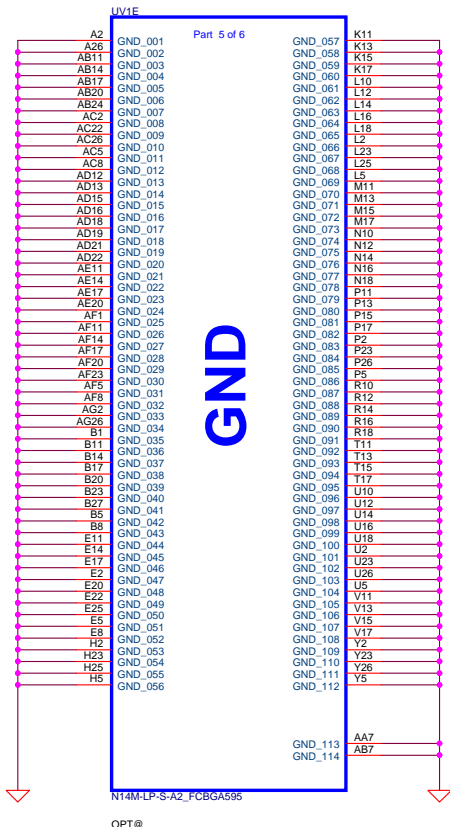
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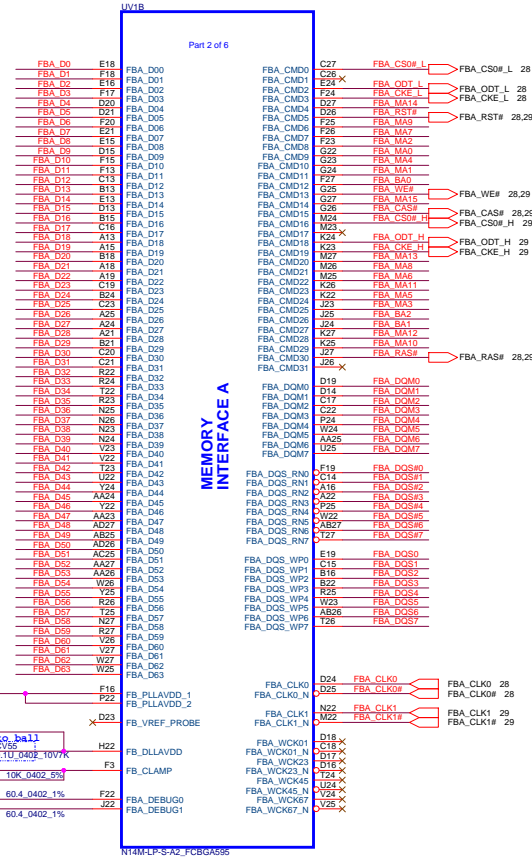
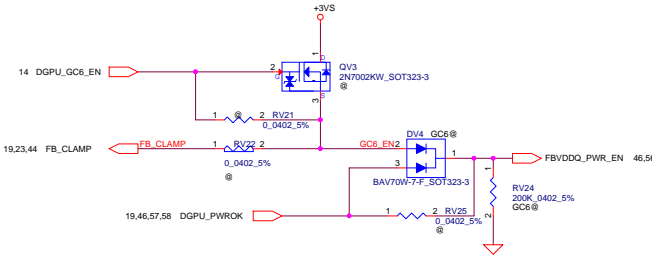
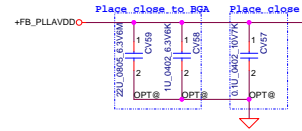
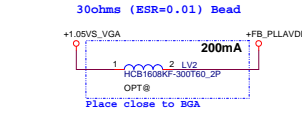
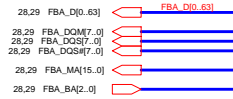
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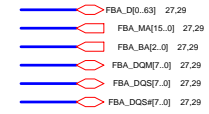
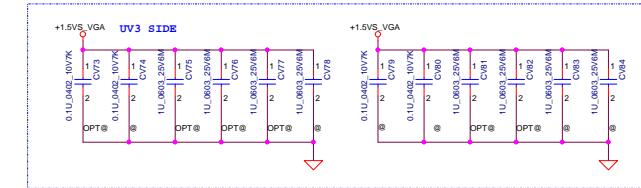
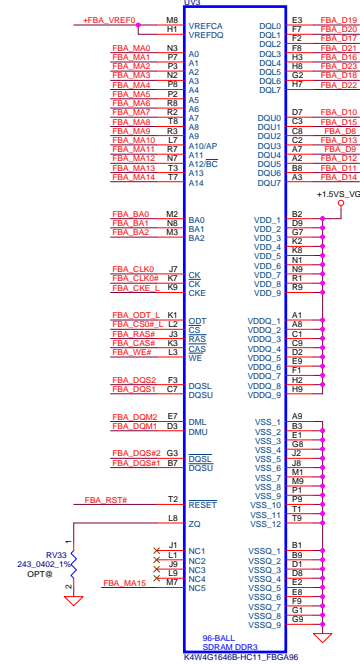
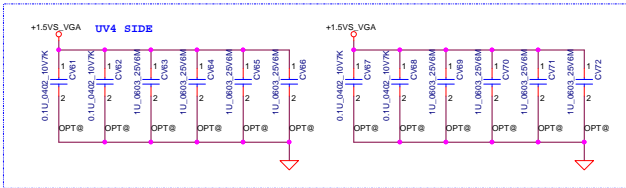
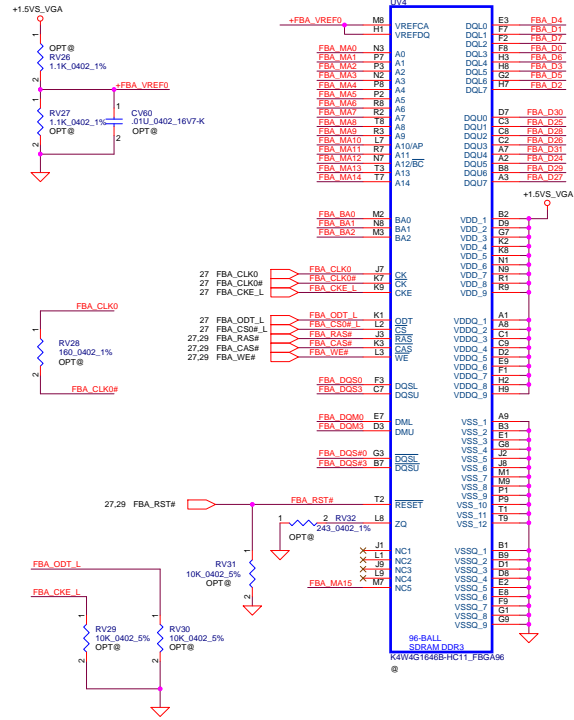
Mode D - Mirror Mode Mapping

Address	DATA Bus
FBX_CMD0	CS0#_L
FBX_CMD1	
FBX_CMD2	ODT_L
FBX_CMD3	CKE_L
FBX_CMD4	A14 A14
FBX_CMD5	RST RST
FBX_CMD6	A9 A9
FBX_CMD7	A7 A7
FBX_CMD8	A2 A2
FBX_CMD9	A0 A0
FBX_CMD10	A4 A4
FBX_CMD11	A1 A1
FBX_CMD12	BA0 BA0
FBX_CMD13	WE# WE#
FBX_CMD14	A15 A15
FBX_CMD15	CAS# CAS#
FBX_CMD16	CS0#_H
FBX_CMD17	
FBX_CMD18	ODT_H
FBX_CMD19	CKE_H
FBX_CMD20	A13 A13
FBX_CMD21	A8 A8
FBX_CMD22	A6 A6
FBX_CMD23	A11 A11
FBX_CMD24	A5 A5
FBX_CMD25	A3 A3
FBX_CMD26	BA2 BA2
FBX_CMD27	BA1 BA1
FBX_CMD28	A12 A12
FBX_CMD29	A10 A10
FBX_CMD30	RAS# RAS#



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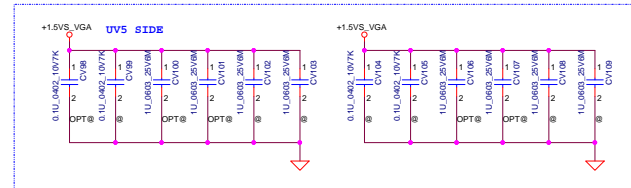
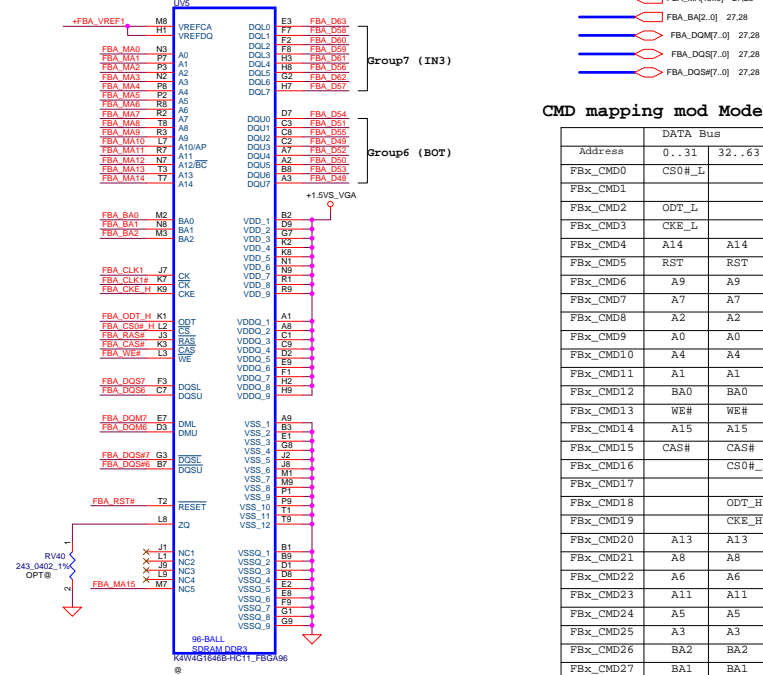
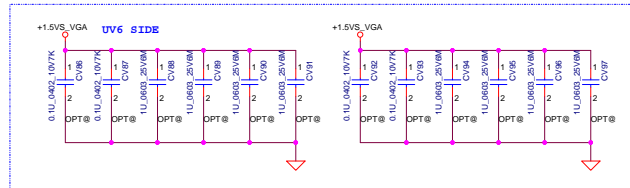
at least 16 mils width(optimal)
20 mils spacing to other signals /planes




CMD mapping mod Mode D

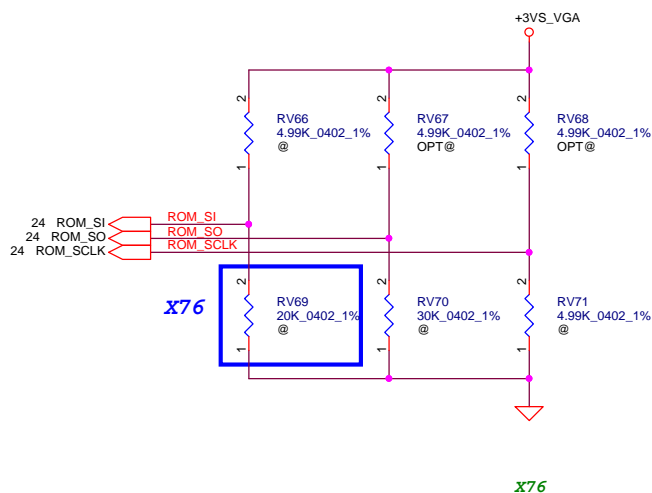
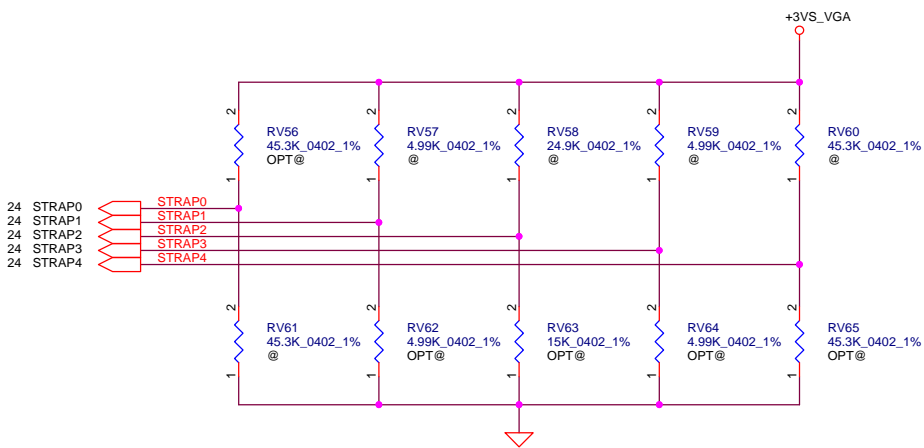
Address	DATA Bus
Fbx_CMD0	0...31 32...63
Fbx_CMD1	CS0#_L
Fbx_CMD2	ODT_L
Fbx_CMD3	CKE_L
Fbx_CMD4	A14 A14
Fbx_CMD5	RST RST
Fbx_CMD6	A9 A9
Fbx_CMD7	A7 A7
Fbx_CMD8	A2 A2
Fbx_CMD9	A0 A0
Fbx_CMD10	A4 A4
Fbx_CMD11	A1 A1
Fbx_CMD12	BA0 BA0
Fbx_CMD13	WE# WE#
Fbx_CMD14	A15 A15
Fbx_CMD15	CAS# CAS#
Fbx_CMD16	CS0#_H
Fbx_CMD17	
Fbx_CMD18	ODT_H
Fbx_CMD19	CKE_H
Fbx_CMD20	A13 A13
Fbx_CMD21	A8 A8
Fbx_CMD22	A6 A6
Fbx_CMD23	A11 A11
Fbx_CMD24	A5 A5
Fbx_CMD25	A3 A3
Fbx_CMD26	BA2 BA2
Fbx_CMD27	BA1 BA1
Fbx_CMD28	A12 A12
Fbx_CMD29	A10 A10
Fbx_CMD30	RAS# RAS#

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[illegible]

	DATA Bus		
Address	0..31	32..63	
Fbx_CMD0	C50#_L		
Fbx_CMD1			
Fbx_CMD2	ODT_L		
Fbx_CMD3	CKE_L		
Fbx_CMD4	A14	A14	
Fbx_CMD5	RST	RST	
Fbx_CMD6	A9	A9	
Fbx_CMD7	A7	A7	
Fbx_CMD8	A2	A2	
Fbx_CMD9	A0	A0	
Fbx_CMD10	A4	A4	
Fbx_CMD11	A1	A1	
Fbx_CMD12	BA0	BA0	
Fbx_CMD13	WE#	WE#	
Fbx_CMD14	A15	A15	
Fbx_CMD15	CAS#	CAS#	
Fbx_CMD16		C50#_H	
Fbx_CMD17			
Fbx_CMD18		ODT_H	
Fbx_CMD19		CKE_H	
Fbx_CMD20	A13	A13	
Fbx_CMD21	A8	A8	
Fbx_CMD22	A6	A6	
Fbx_CMD23	A11	A11	
Fbx_CMD24	A5	A5	
Fbx_CMD25	A3	A3	
Fbx_CMD26	BA2	BA2	
Fbx_CMD27	BA1	BA1	
Fbx_CMD28	A12	A12	
Fbx_CMD29	A10	A10	
Fbx_CMD30	RAS#	RAS#	

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

USER Straps	
User[3:0]	
1000-1100	Customer defined

DP_PLL_VDD33V	
0	Reserved
1	Default

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

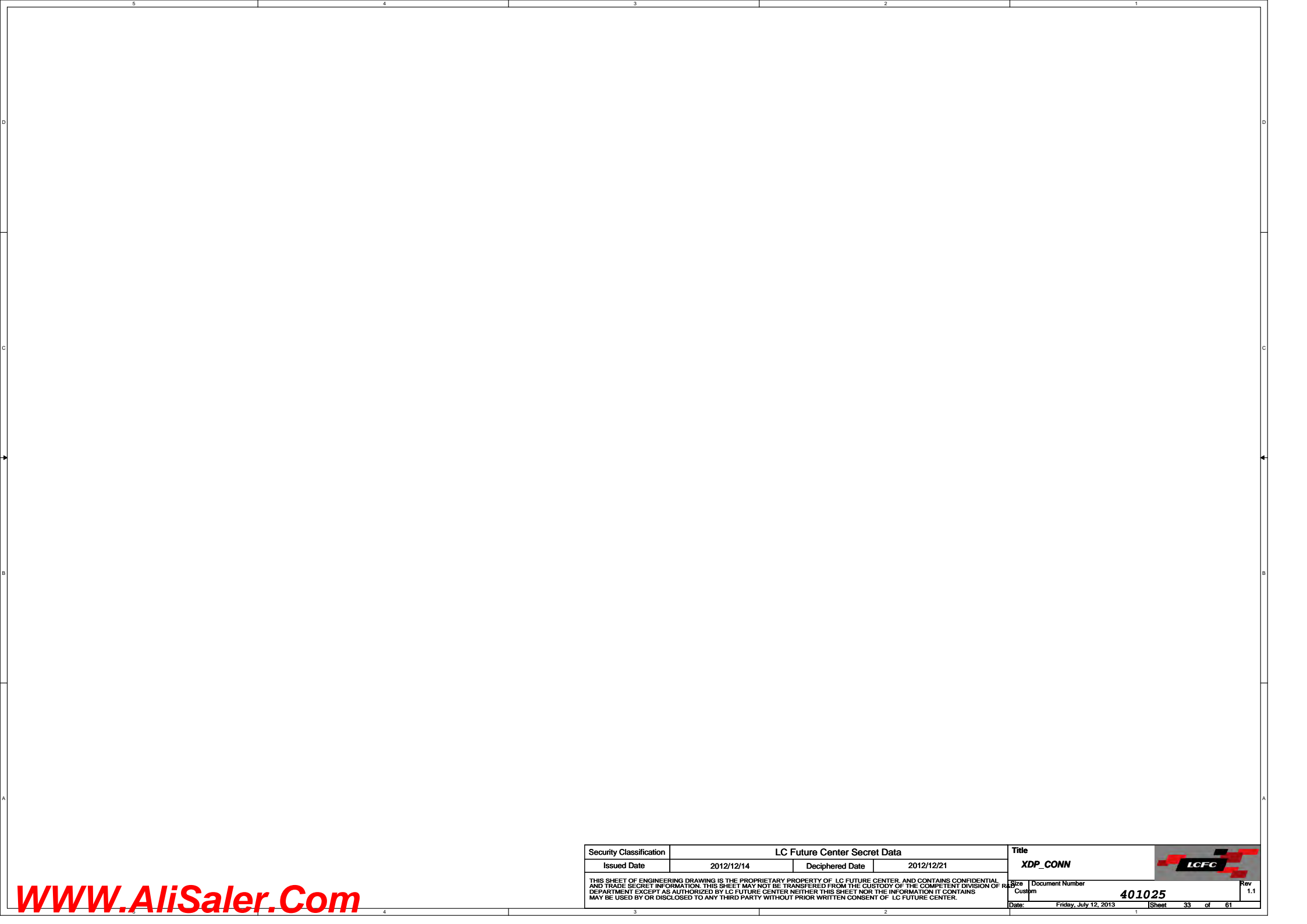
GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV2	Samsung 1GHz	K4W2G1646E-BC1A	0x7	PU 4.99K	PU 4.99K	PU 45.3K	PD 4.99K	PD 15K	PD 4.99K	PU 45.3K
		128M x 16	PD 45.3K							
	Micron 1GMHz	MT41J128M16JT-093G:K	0x5							
		128M x 16	PD 30.1K							
	Hynix 1GMHz	H5TC2G63FFR-11C	0x4							
		128M x 16	PD 24.9K							
	Samsung 900MHz	K4W4G1646B-HC11	0x3							
		256M x 16	PD 20K							
	Micron 900MHz	MT41K256M16HA-107G:E	0x1							
		256M x 16	PD 10K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		


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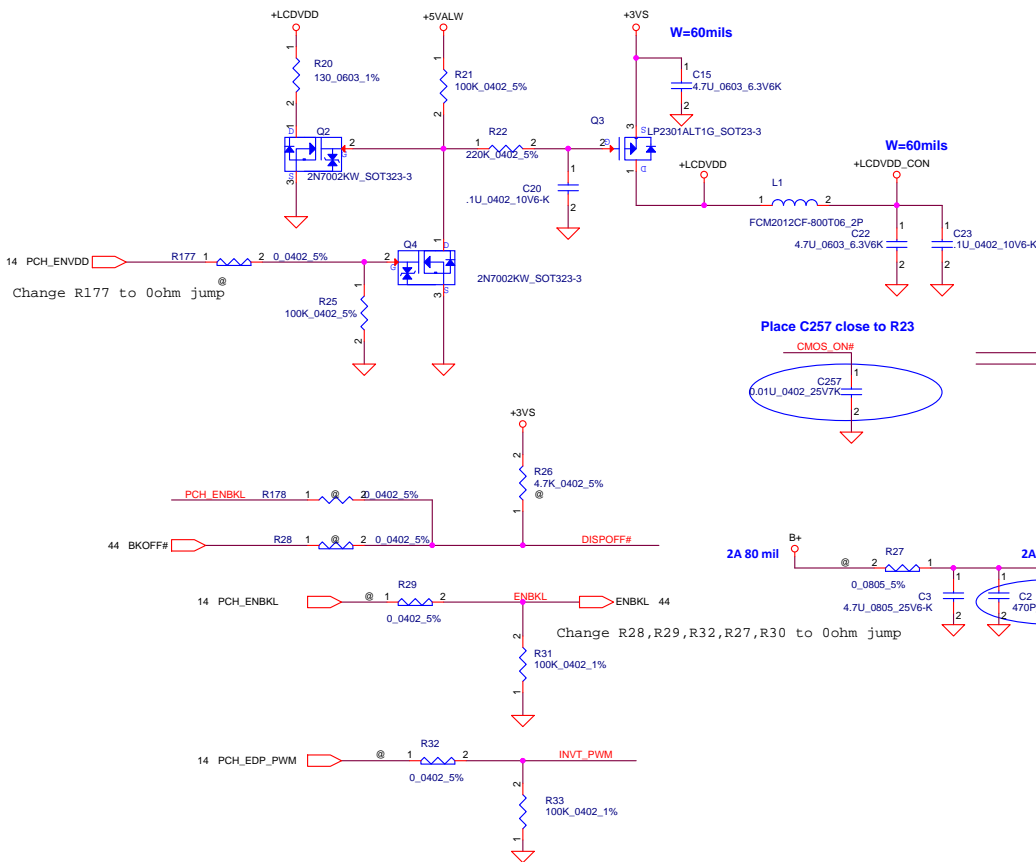
Rev 1.1



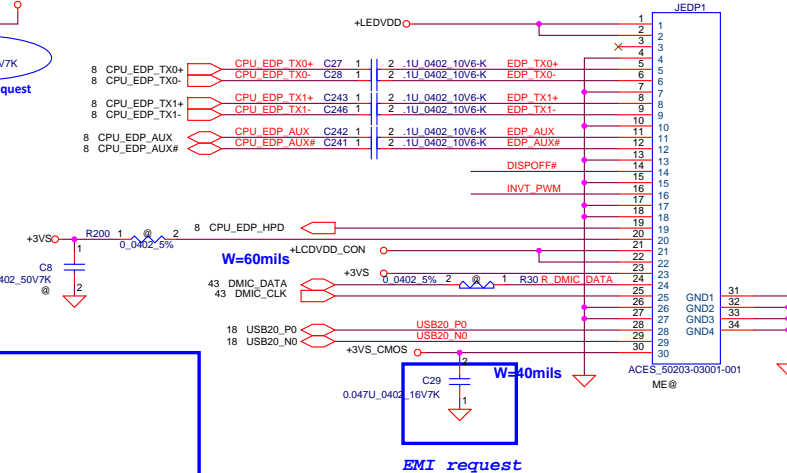
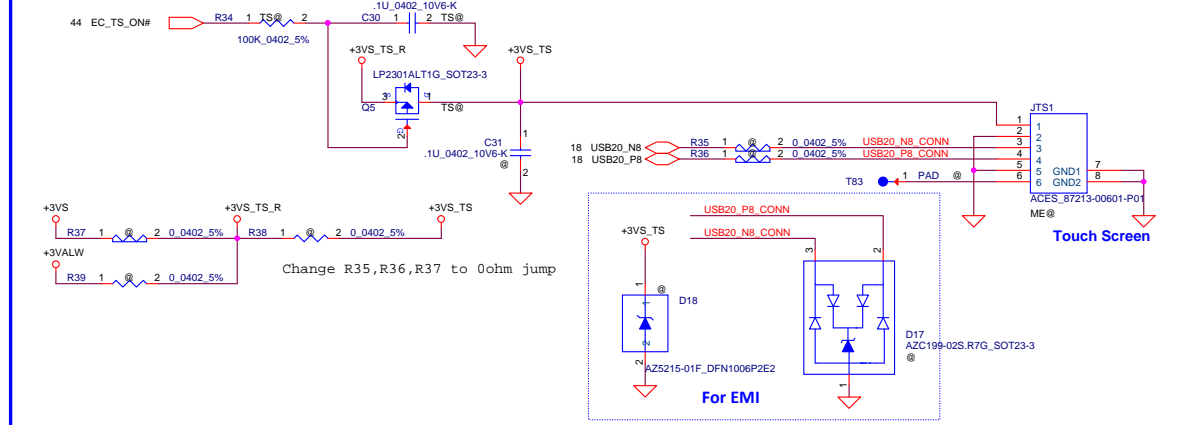
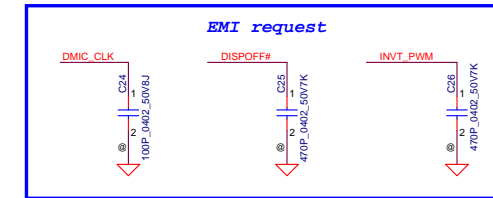
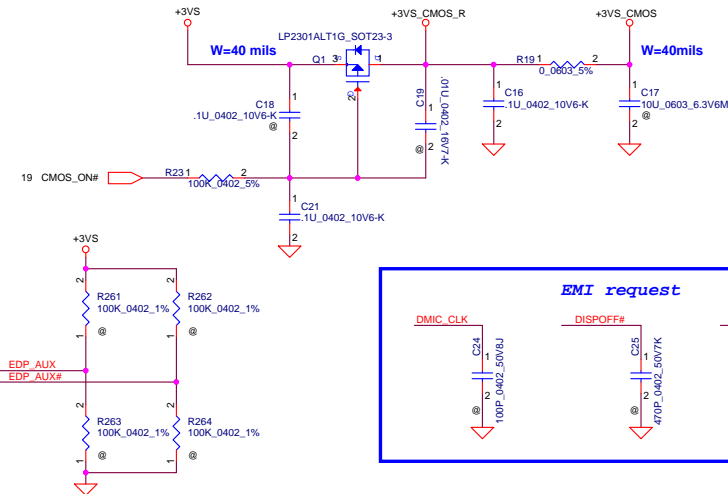
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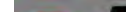
LCD POWER CIRCUIT

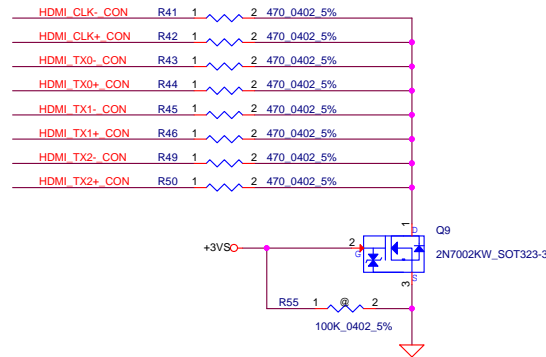
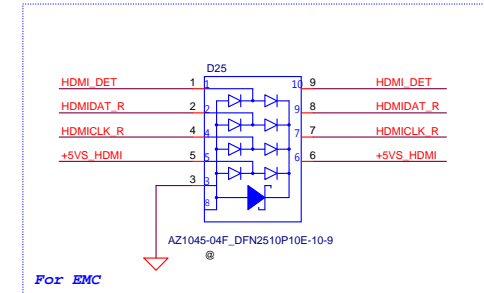
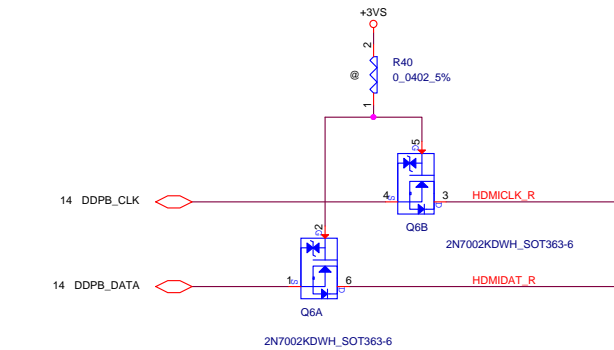
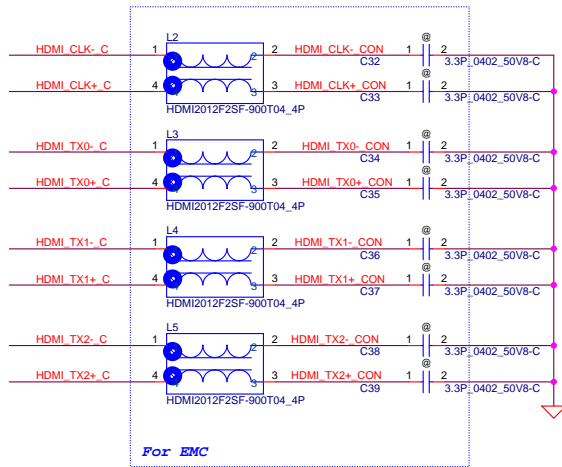


CMOS Camera

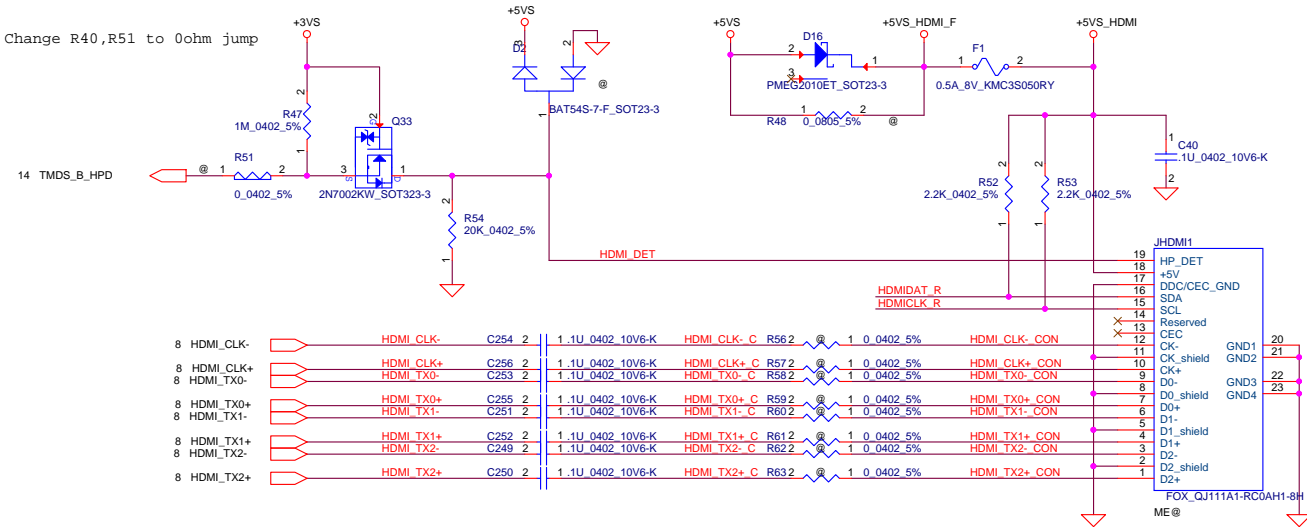


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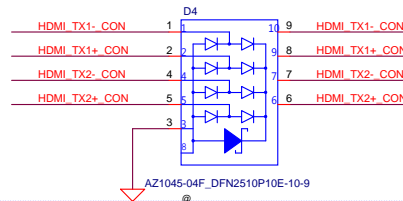
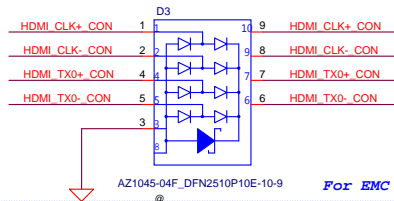
Title			
eDP/ CMOS/Touch screen			
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Change R40,R51 to 0ohm jump

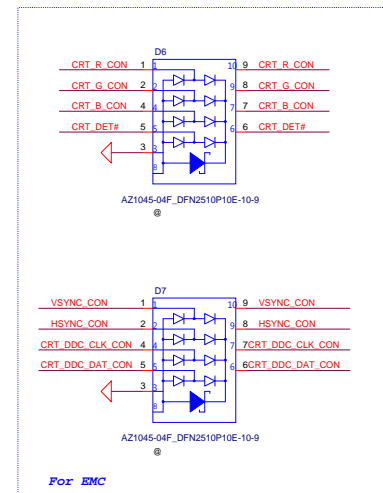
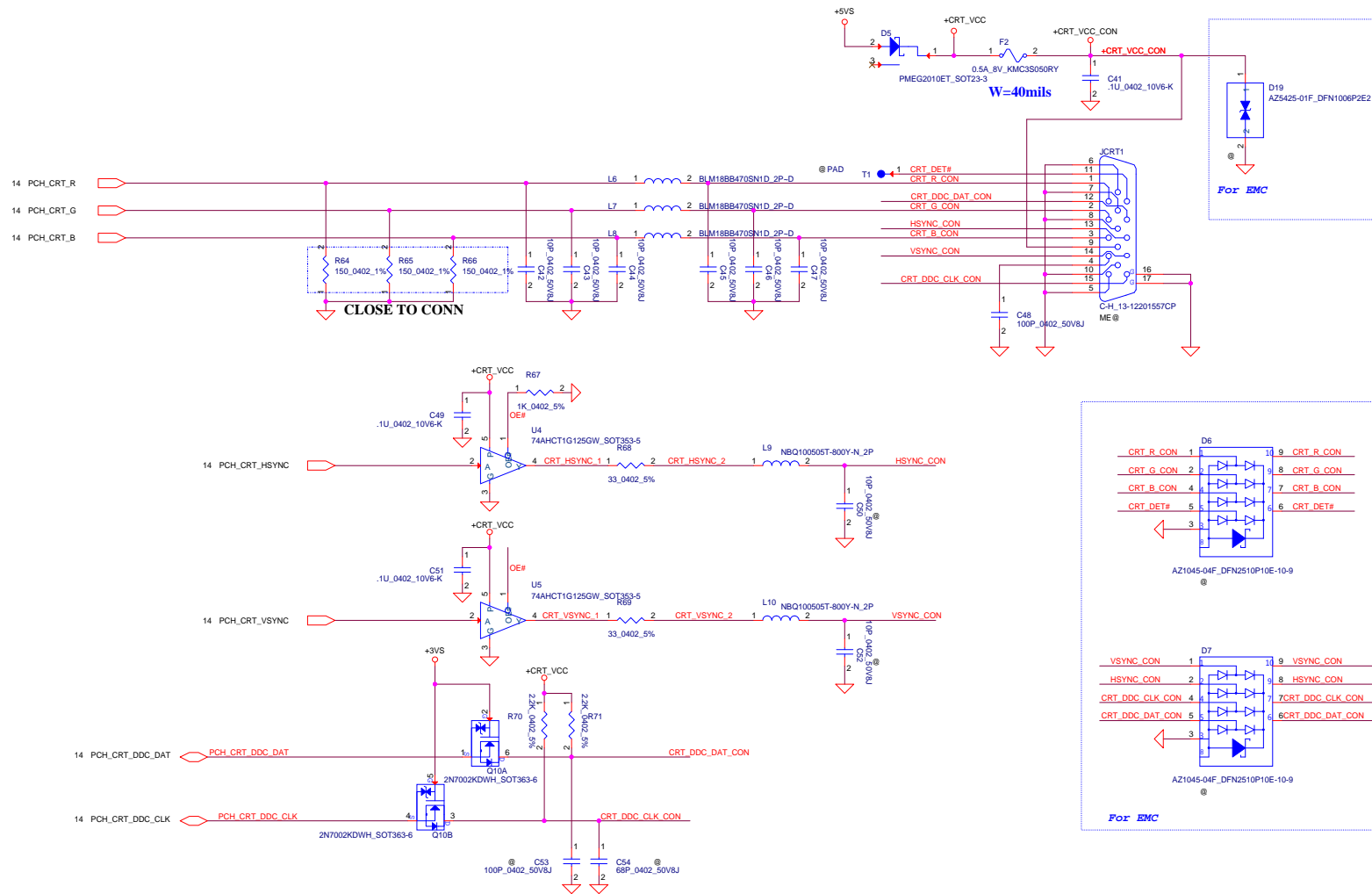


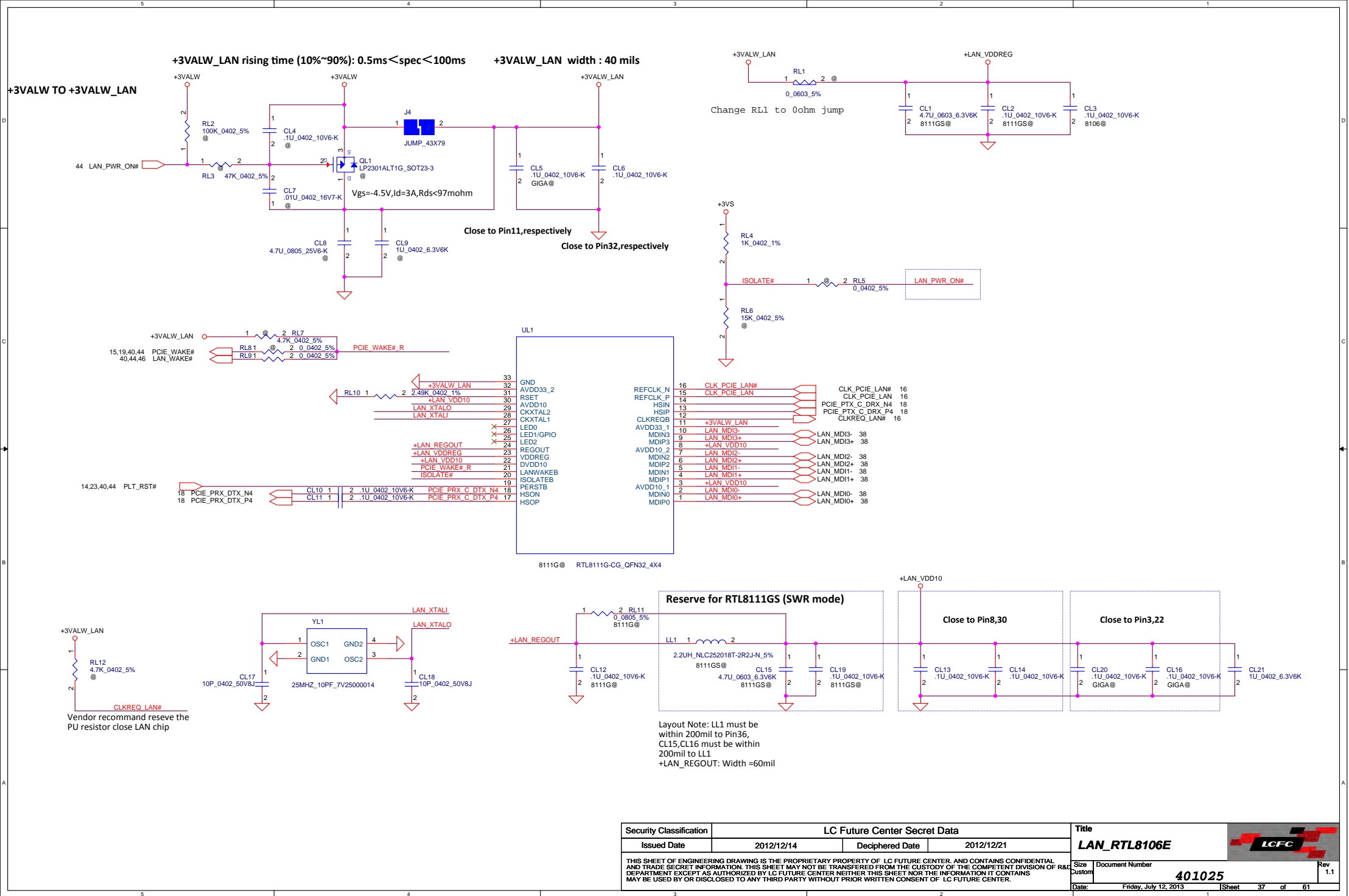
Close to JHDMI1



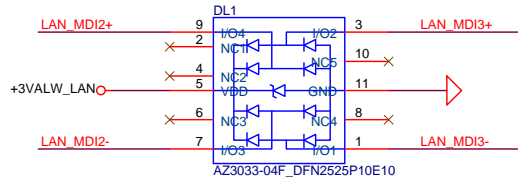
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CRT Connector

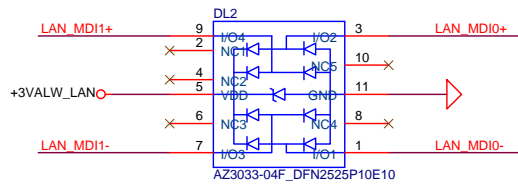




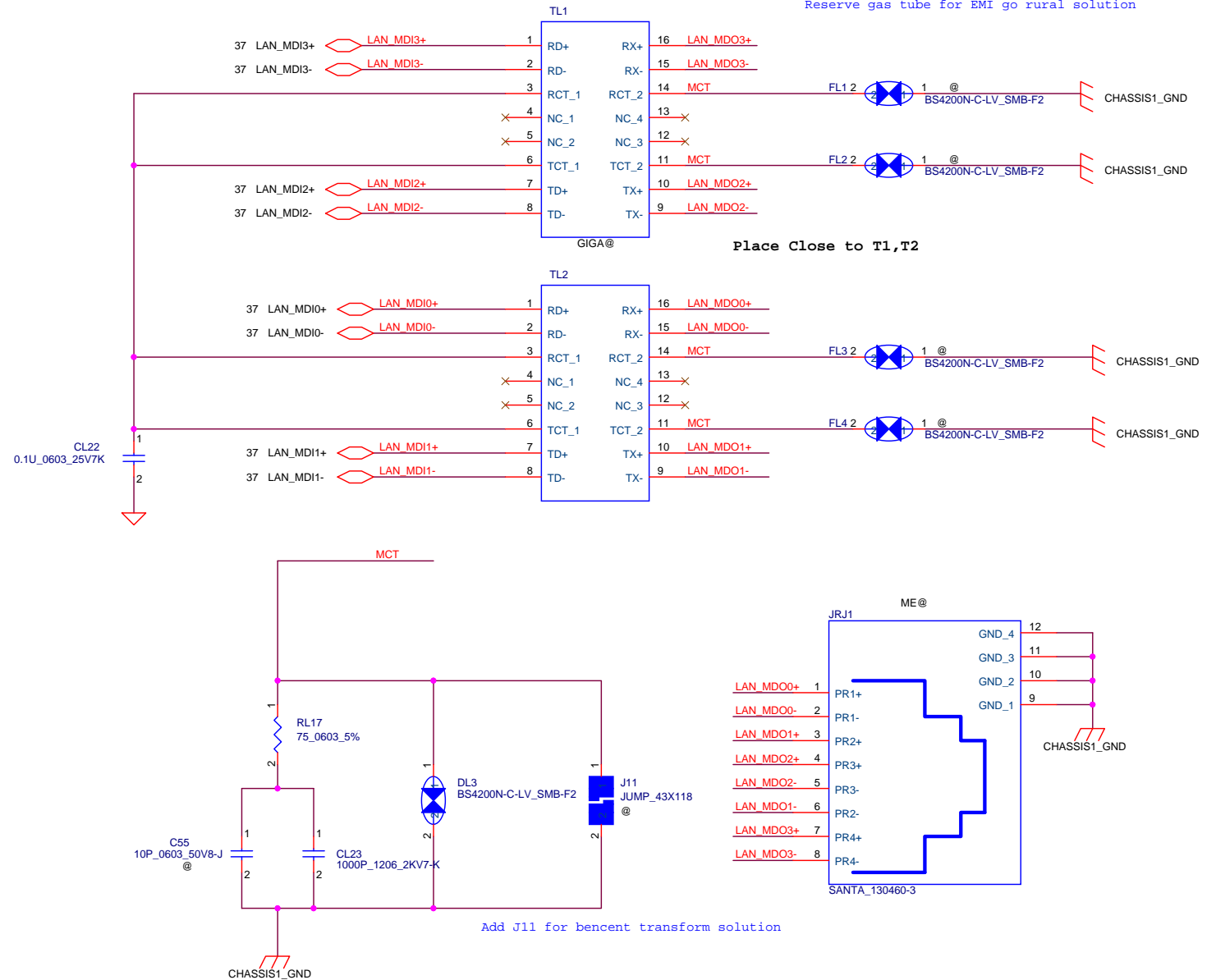
DL1/DL2
1'S PN:SC300003M00



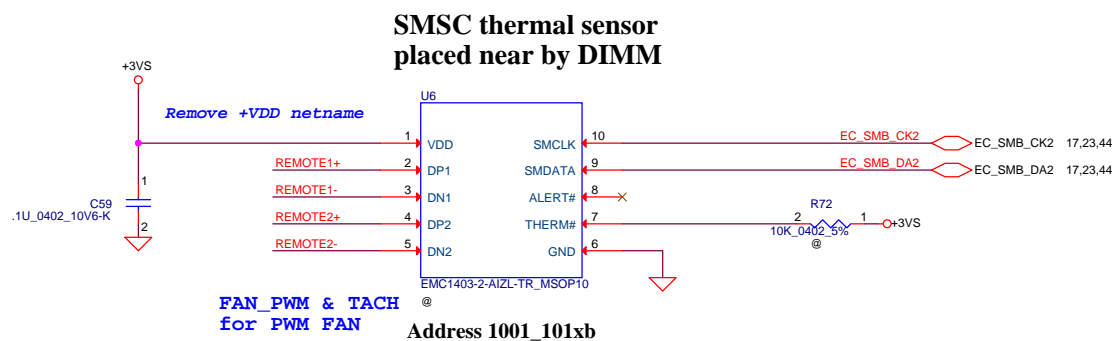
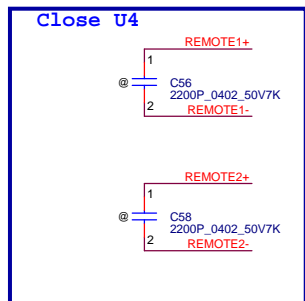
Place Close to TL1



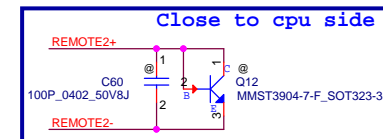
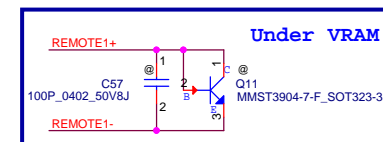
Place Close to TL2



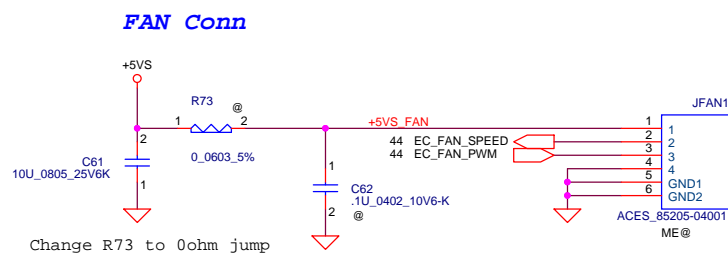
Security Classification	LC Future Center Secret Data			Title	LAN_Transformer	
Issued Date	2012/12/14	Deciphered Date	2012/12/21	Document Number	401025	
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internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

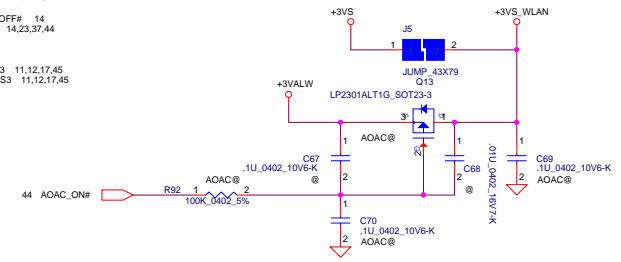


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



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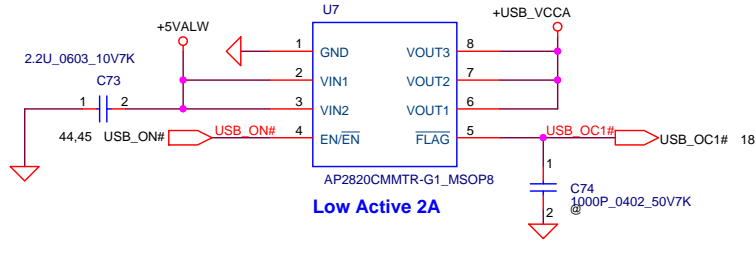
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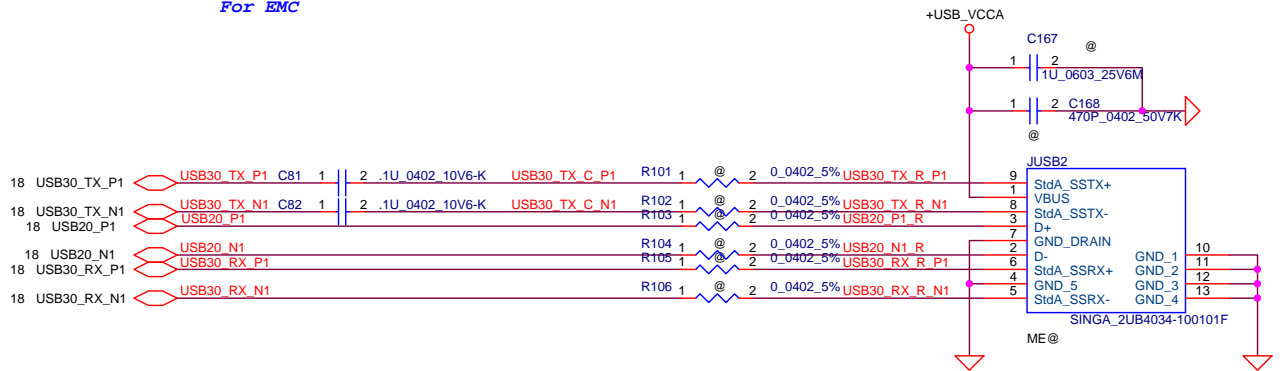
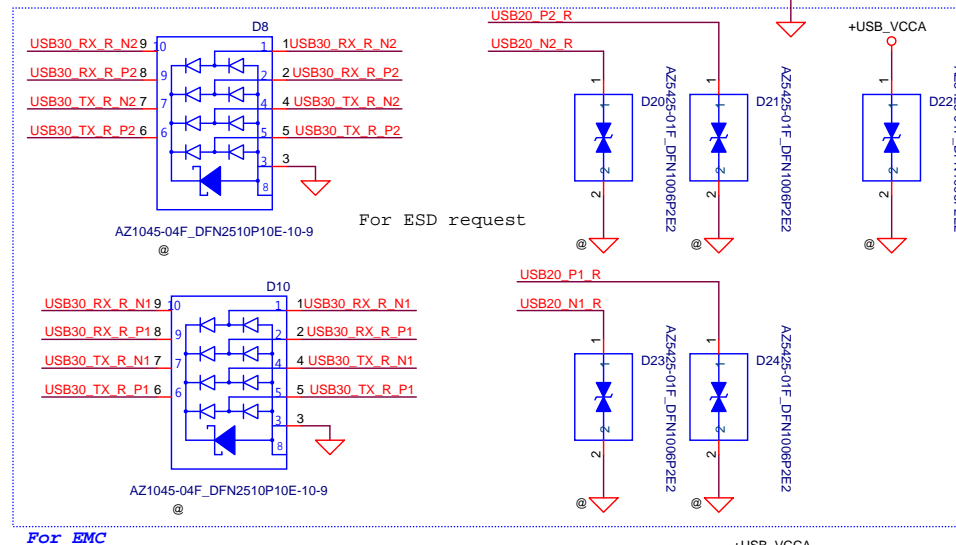
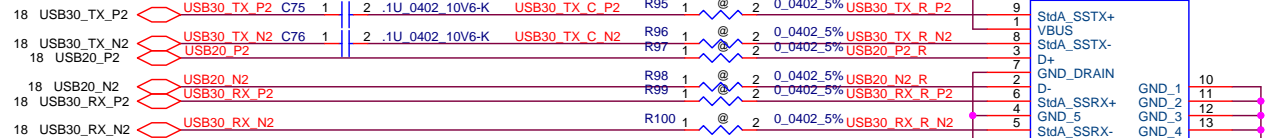
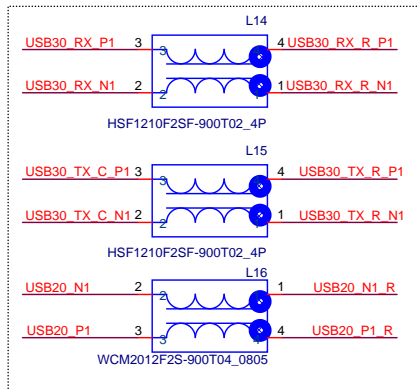
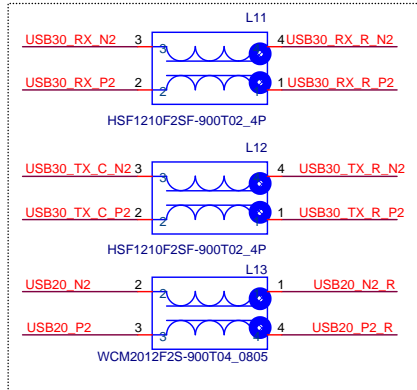
WLAN&BT Combo module circuits


	BT on module Enable	BT on module Disable
* BT_CTRL (GPIO22)	H	L
PCH_BT_ON#	L	H

LEFT SIDE USB3.0 PORT X2

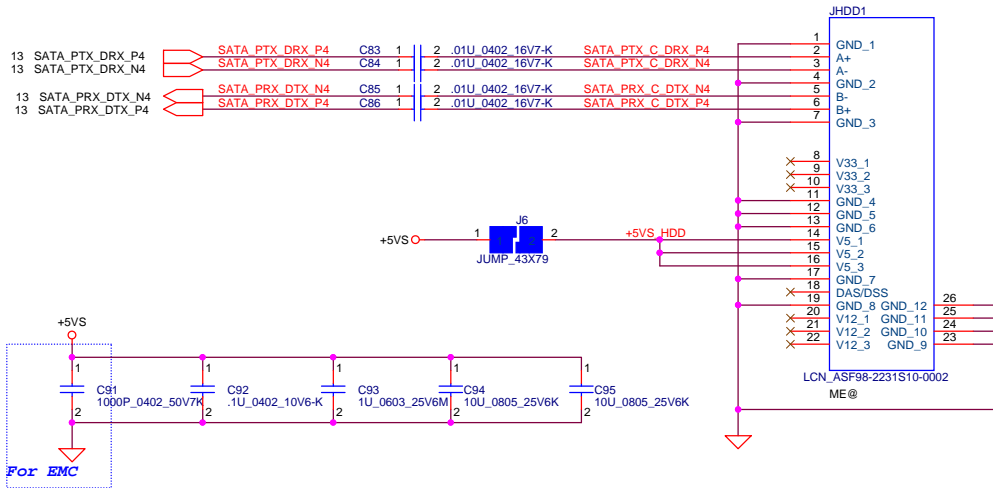


For EMI request
 USB2.0 choke --> SM070001S0J
 USB3.0 Choke --> SM070001S0J

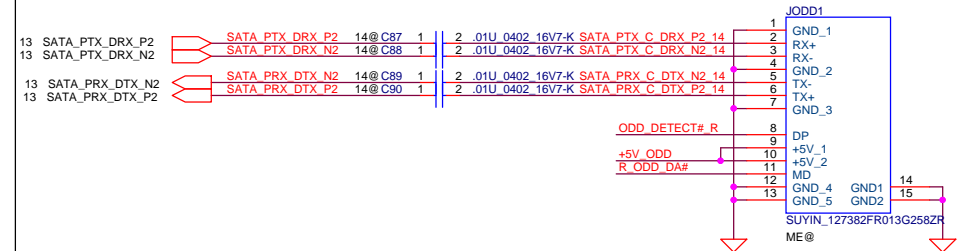


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SATA HDD Conn.

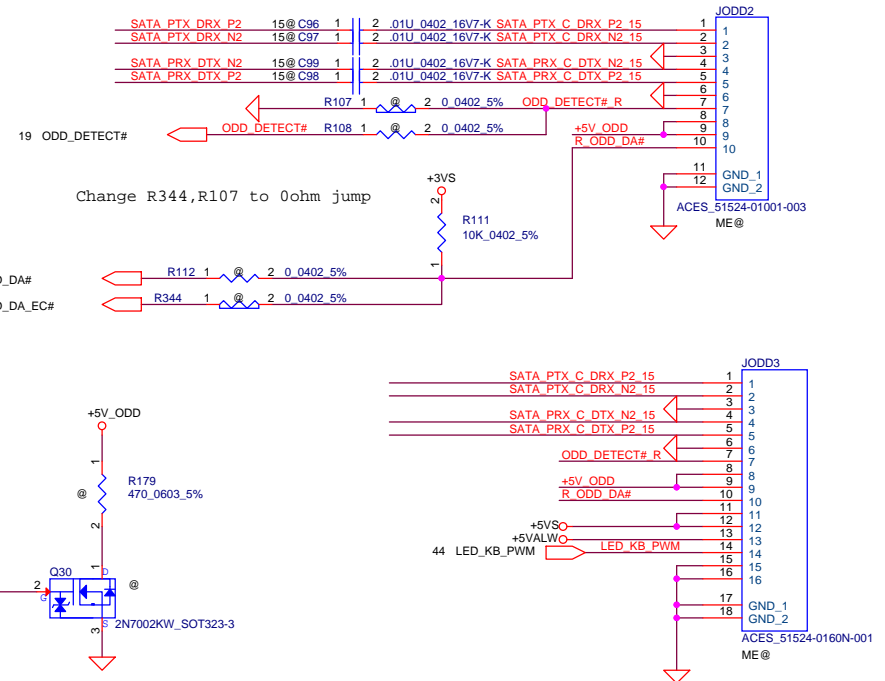



FOR 14" SATA ODD Conn.

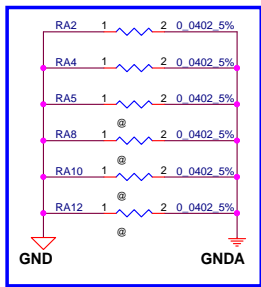


FOR 15"

Co-lay SATA ODD FFC Conn JODD2& JODD3.



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The diagram shows two resistors, RA13 and RA14, connected in parallel between the +1.5VS supply and the AVDD2 pin. Both resistors are labeled with a value of 0.0402 5%.

+5VA
CA4: 10U_0805_10V4Z
CA5: 1U_0402_10V6-K
Place close to Pin 26

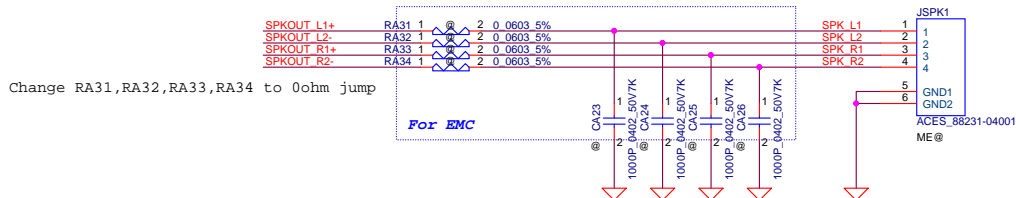
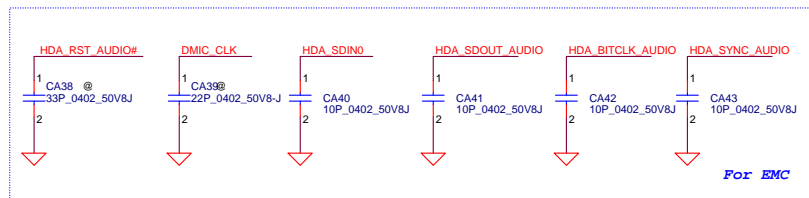
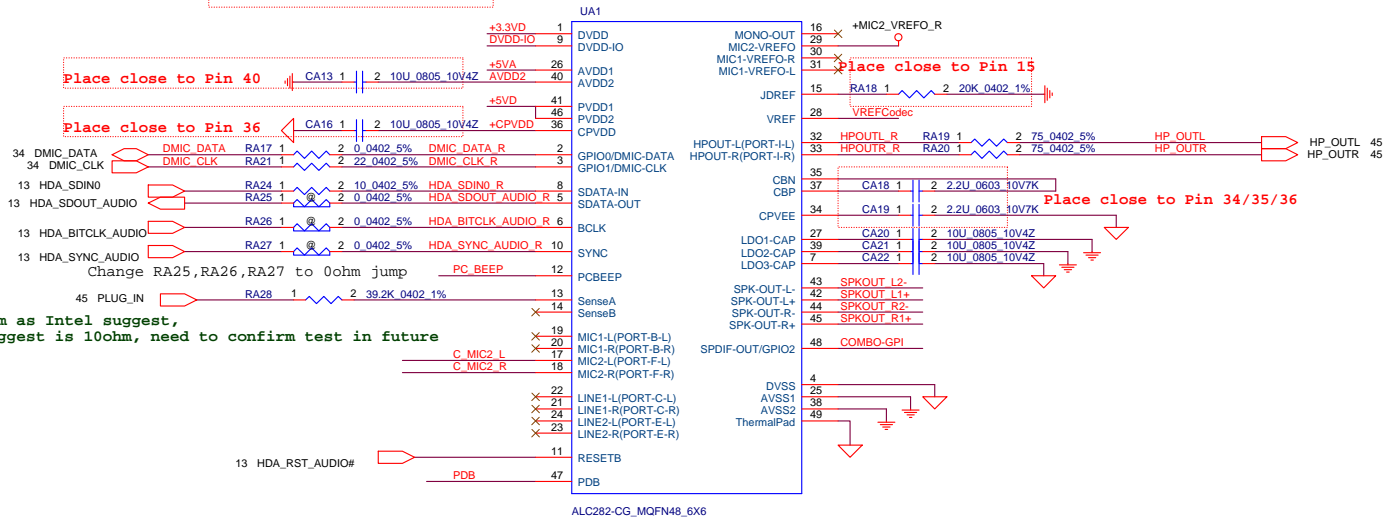
+3.3VD
CA9: 10U_0603_6.3V6M
CA10: 1U_0402_10V6-K
Place close to Pin 1

DVDD-IO
CA1: 10U_0805_10V4Z
CA6: 1U_0402_10V6-K
Place close to pin 9

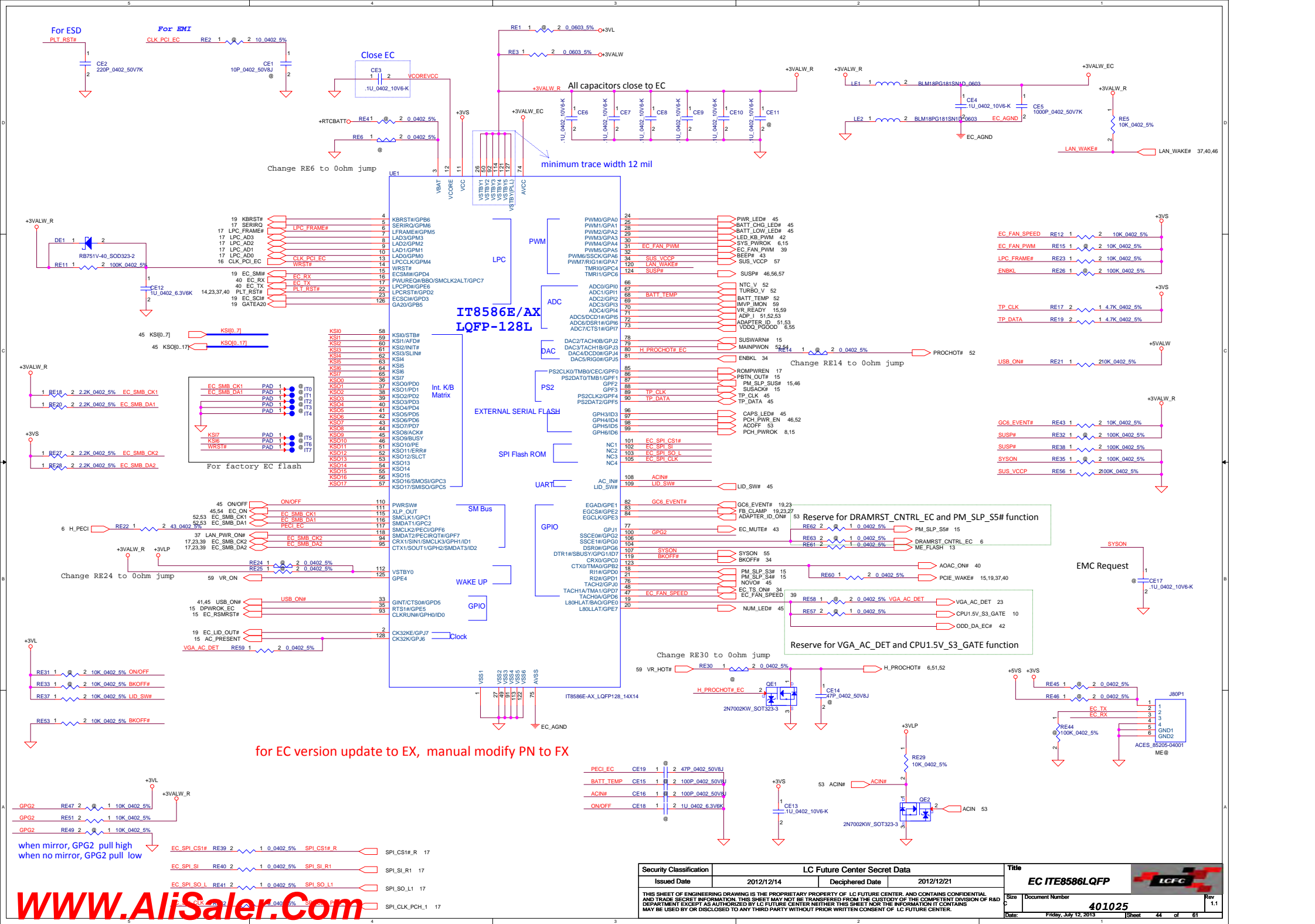
+5VDD
CA2: 10U_0805_10V4Z
CA7: 1U_0402_10V6-K
Place close to Pin 41

+5V
CA8: 10U_0805_10V4Z
CA3: 1U_0402_10V6-K
Place close to Pin 46

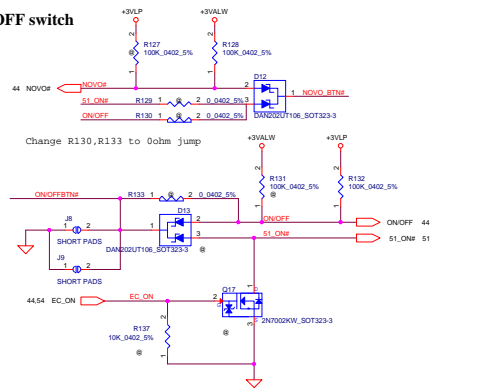
VREFCodec
CA15: 2.2U_0603_6.3V6K
CA44: 1U_0402_10V6-K
Place close to Pin 28



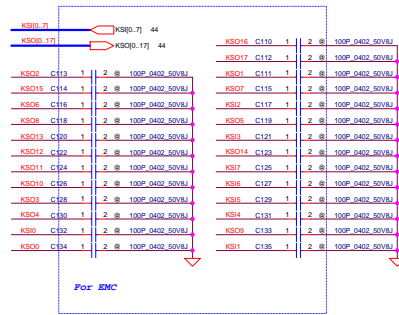
Title			
Audio Codec_ALC282			
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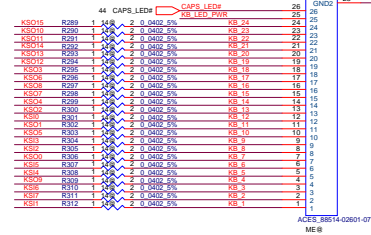
ON/OFF switch



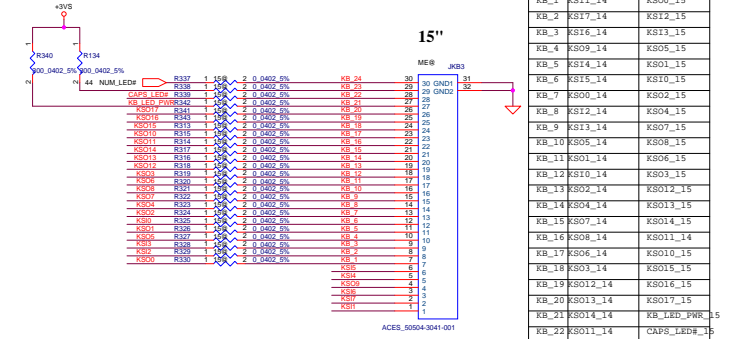
K/B Connector



14"

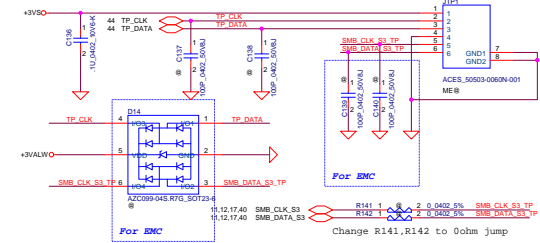


15"

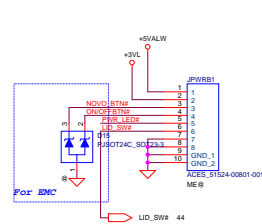


KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS15_14	KS10_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS10_14	KS03_15
KB_13	KS02_14	KS012_15
KB_14	KS04_14	KS013_15
KB_15	KS07_14	KS014_15
KB_16	KS08_14	KS011_15
KB_17	KS06_14	KS010_15
KB_18	KS03_14	KS015_15
KB_19	KS012_14	KS016_15
KB_20	KS014_14	KS017_15
KB_21	KS014_14	KB_LED_PWR_15
KB_22	KS011_14	CAPS_LED#_15
KB_23	KS010_14	VDD_15
KB_24	KS015_14	NOM_LED#_15

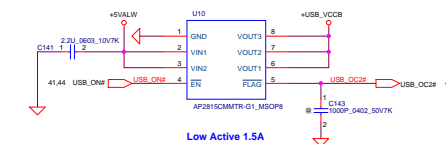
TP/B Connector



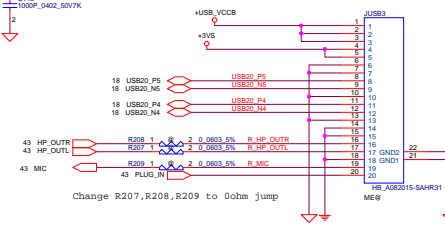
PWR/B Connector



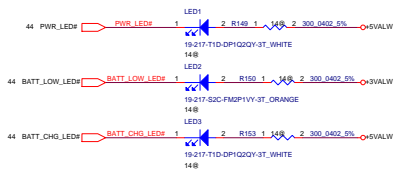
Right Side USB2.0 Port X 1 (USB/B)



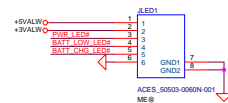
USB I/O Connector



LED (For 14")

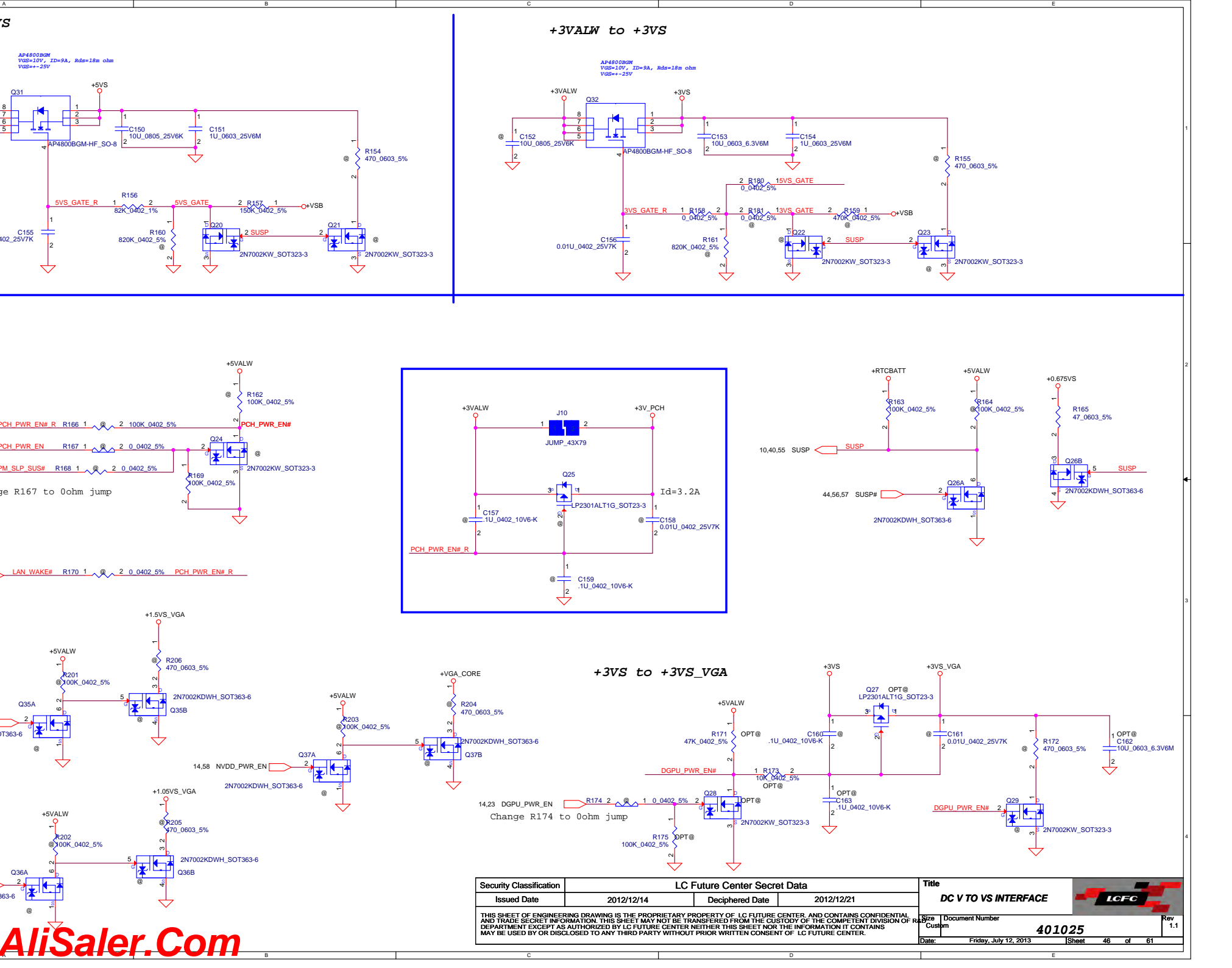
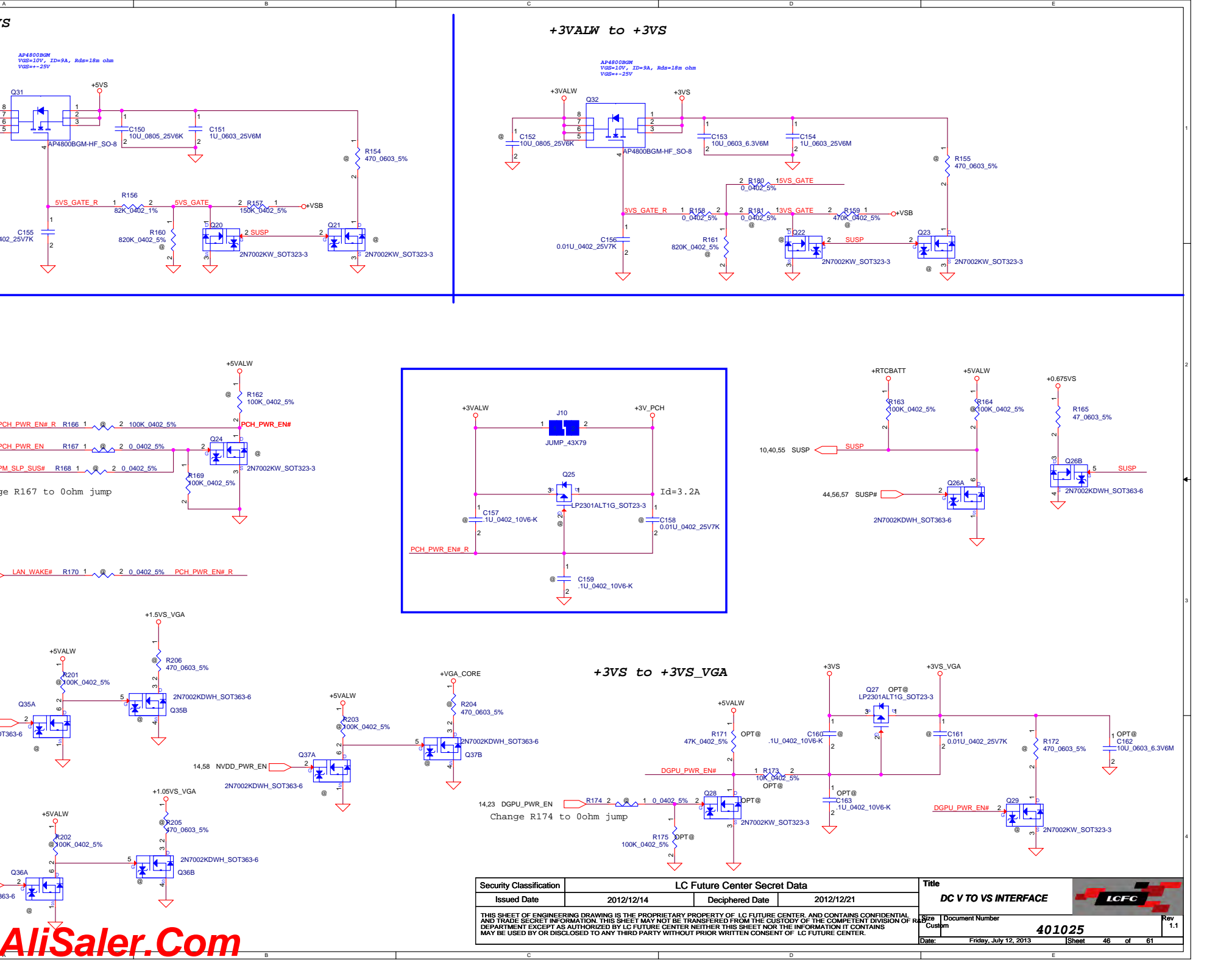
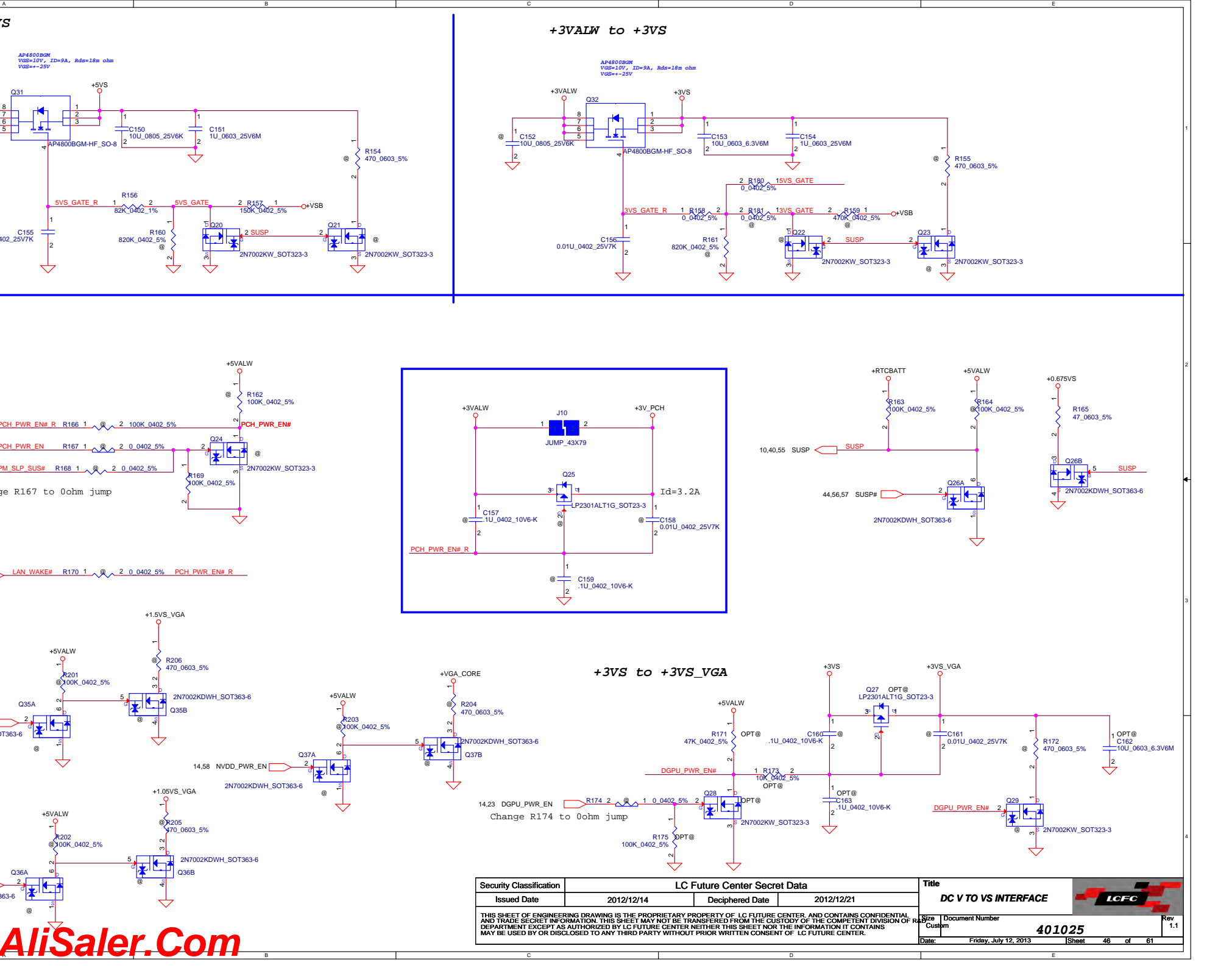
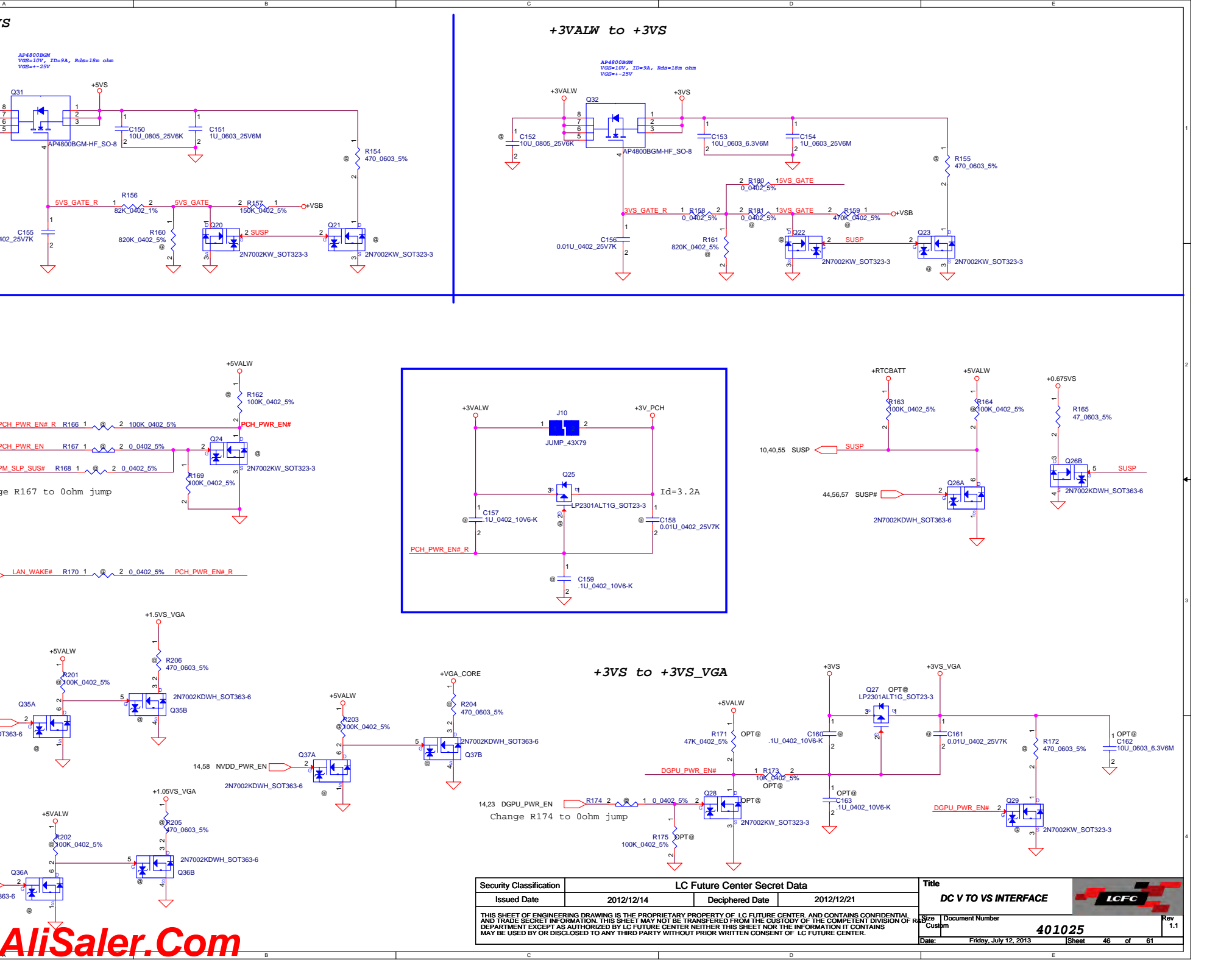
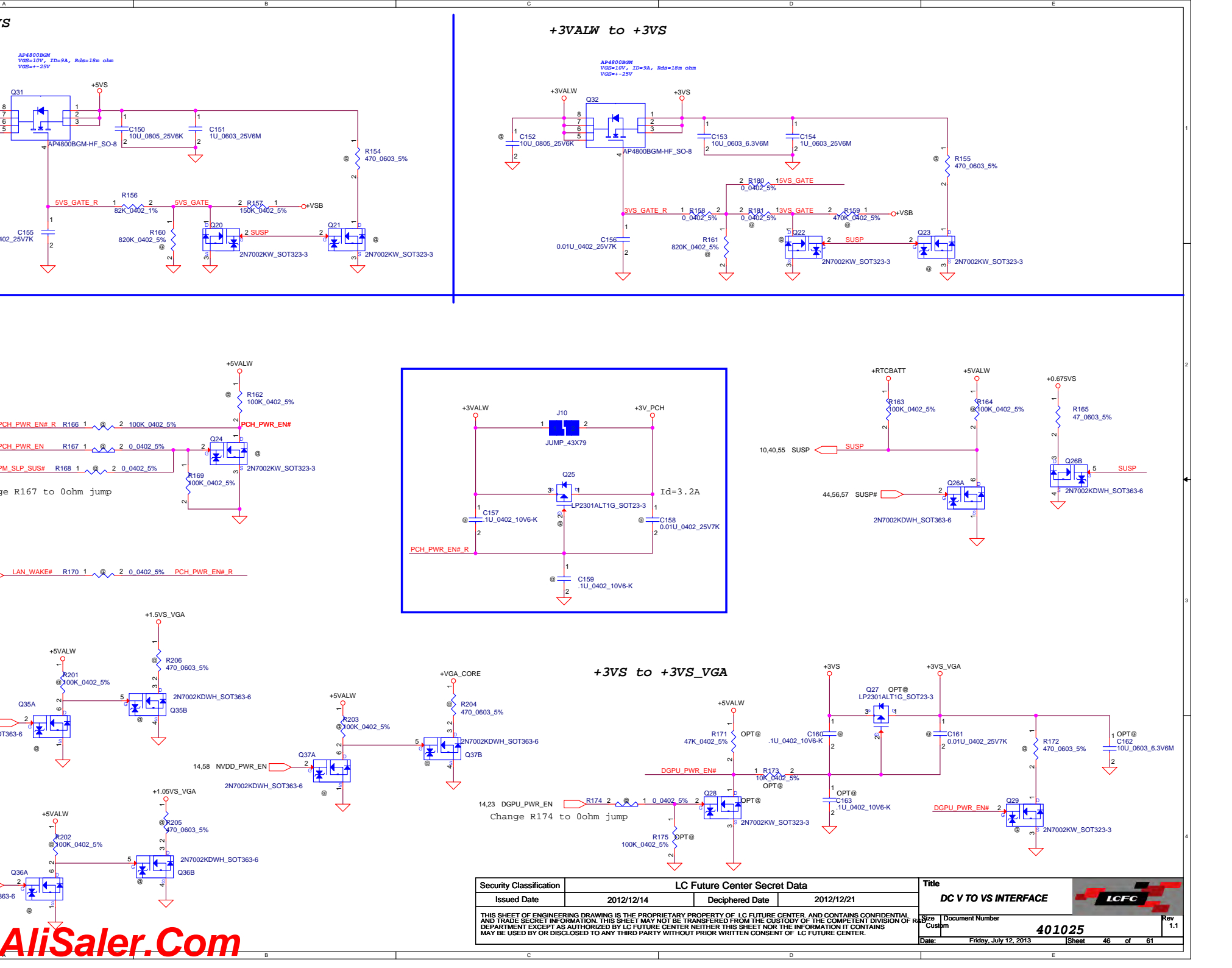
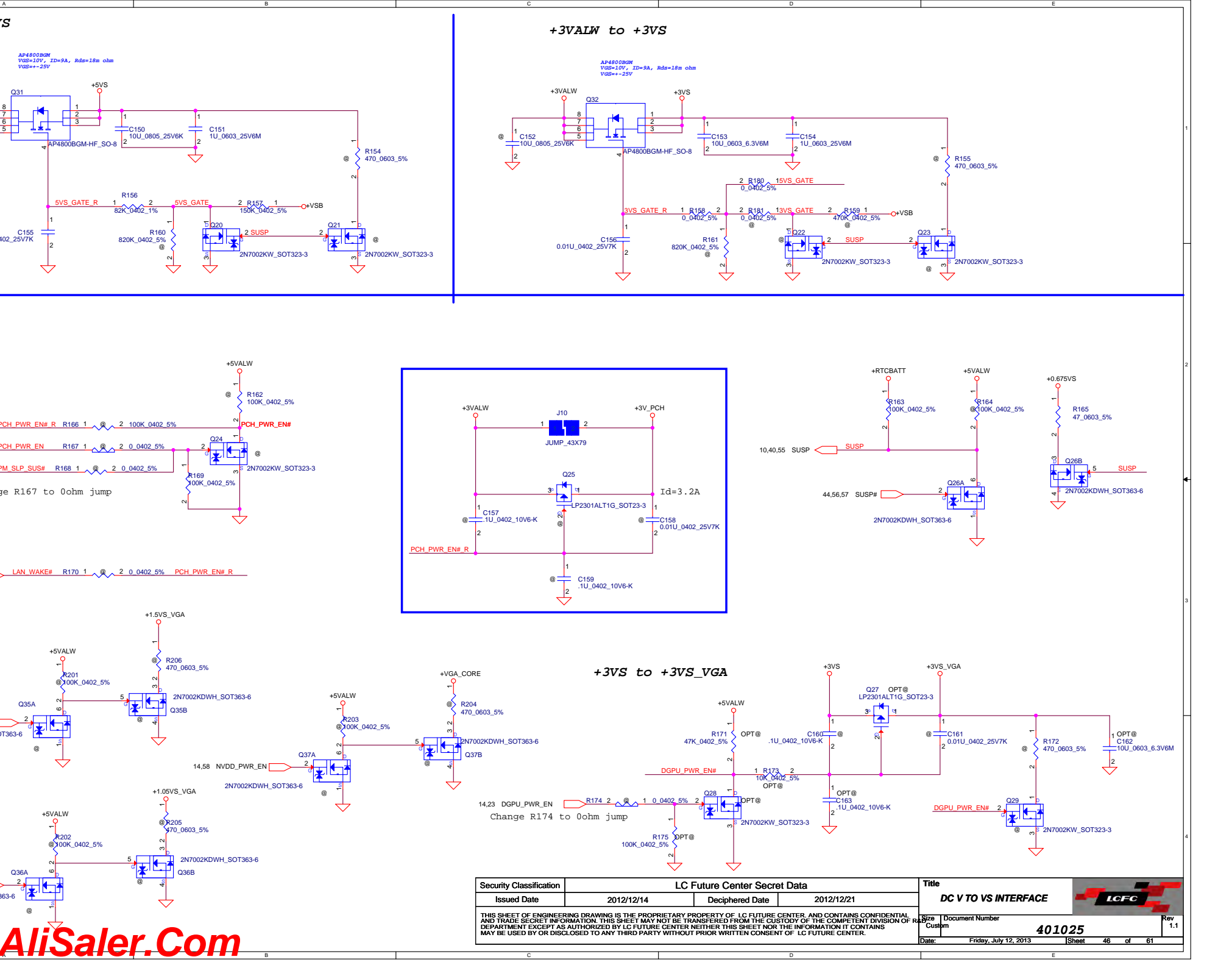
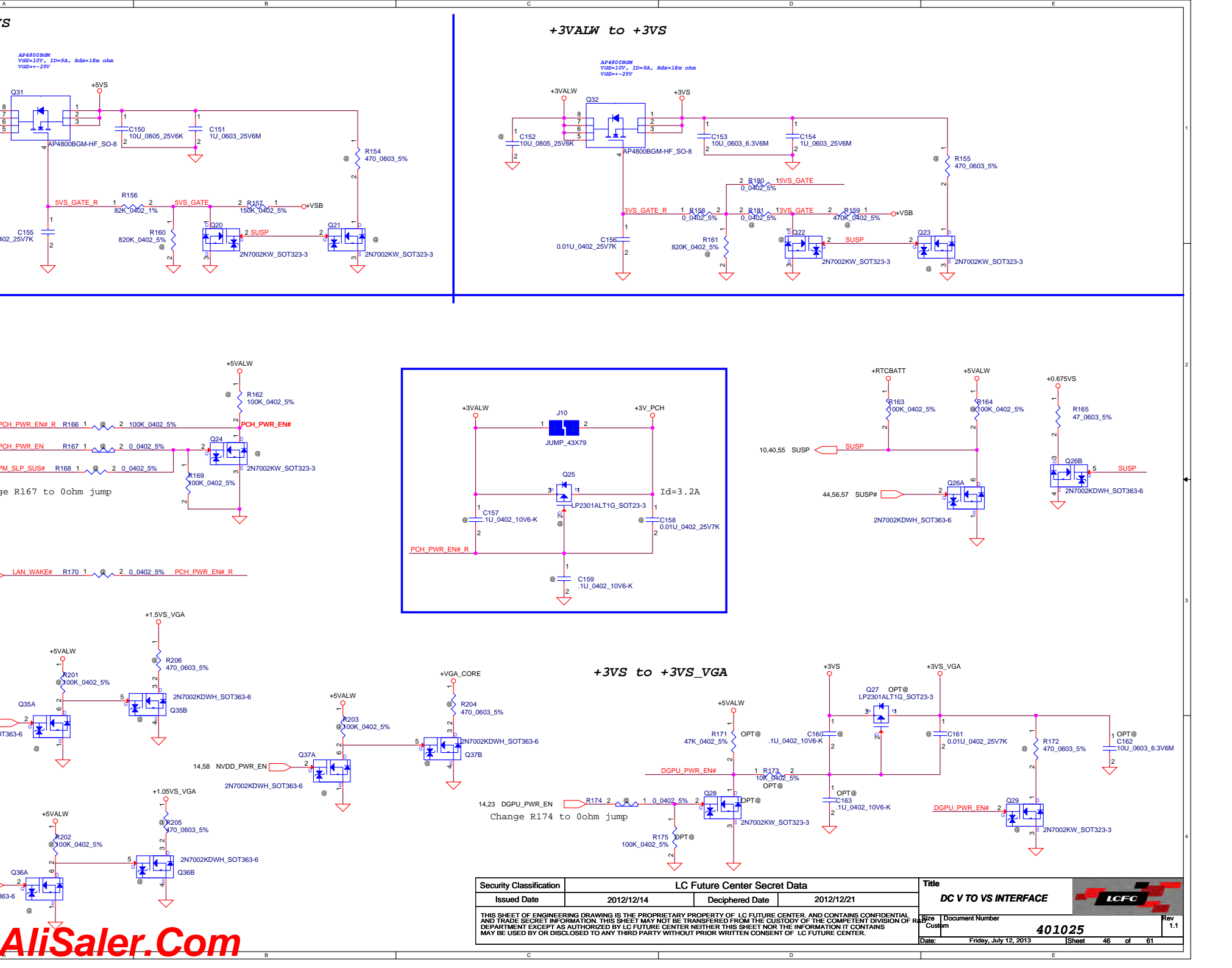
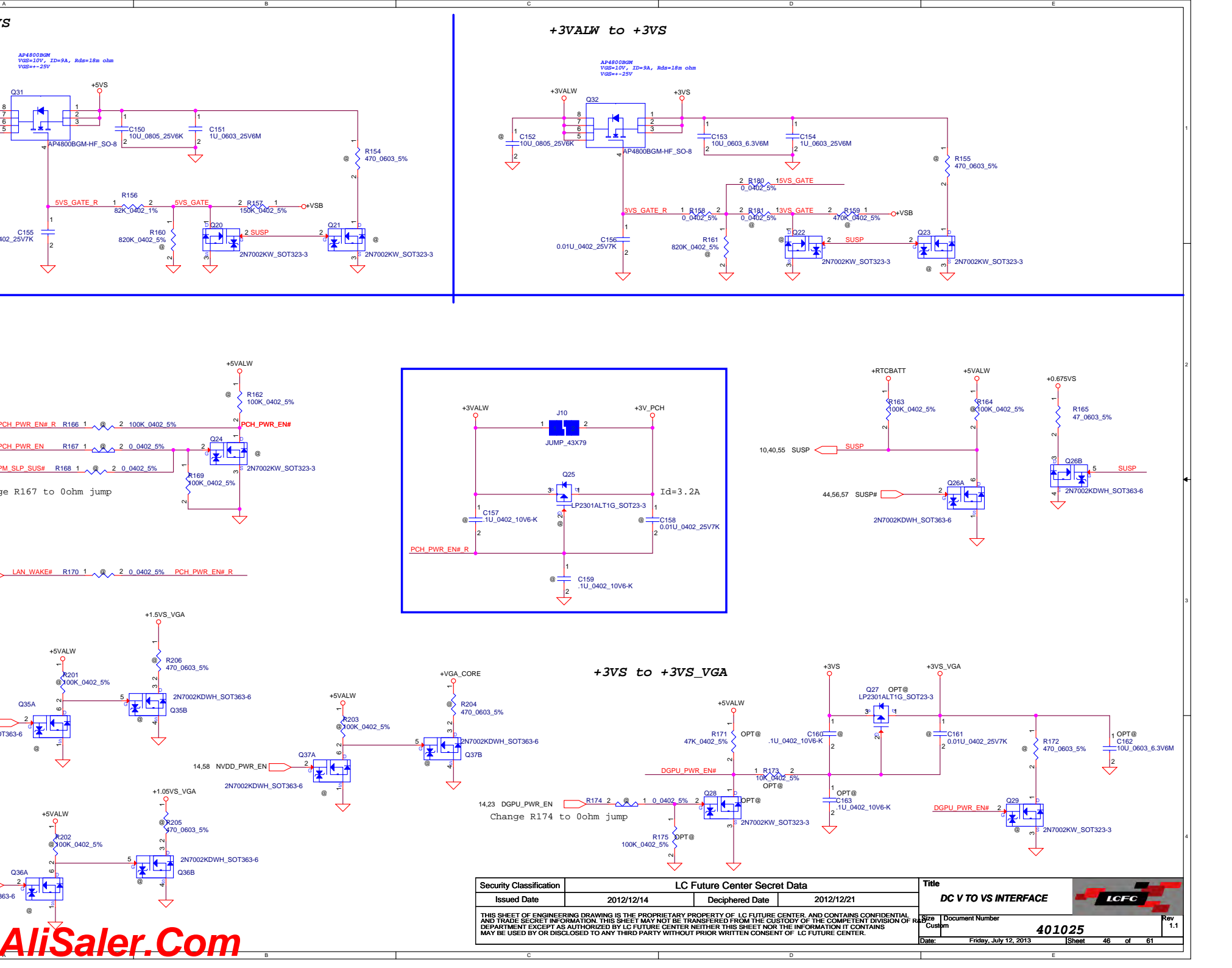


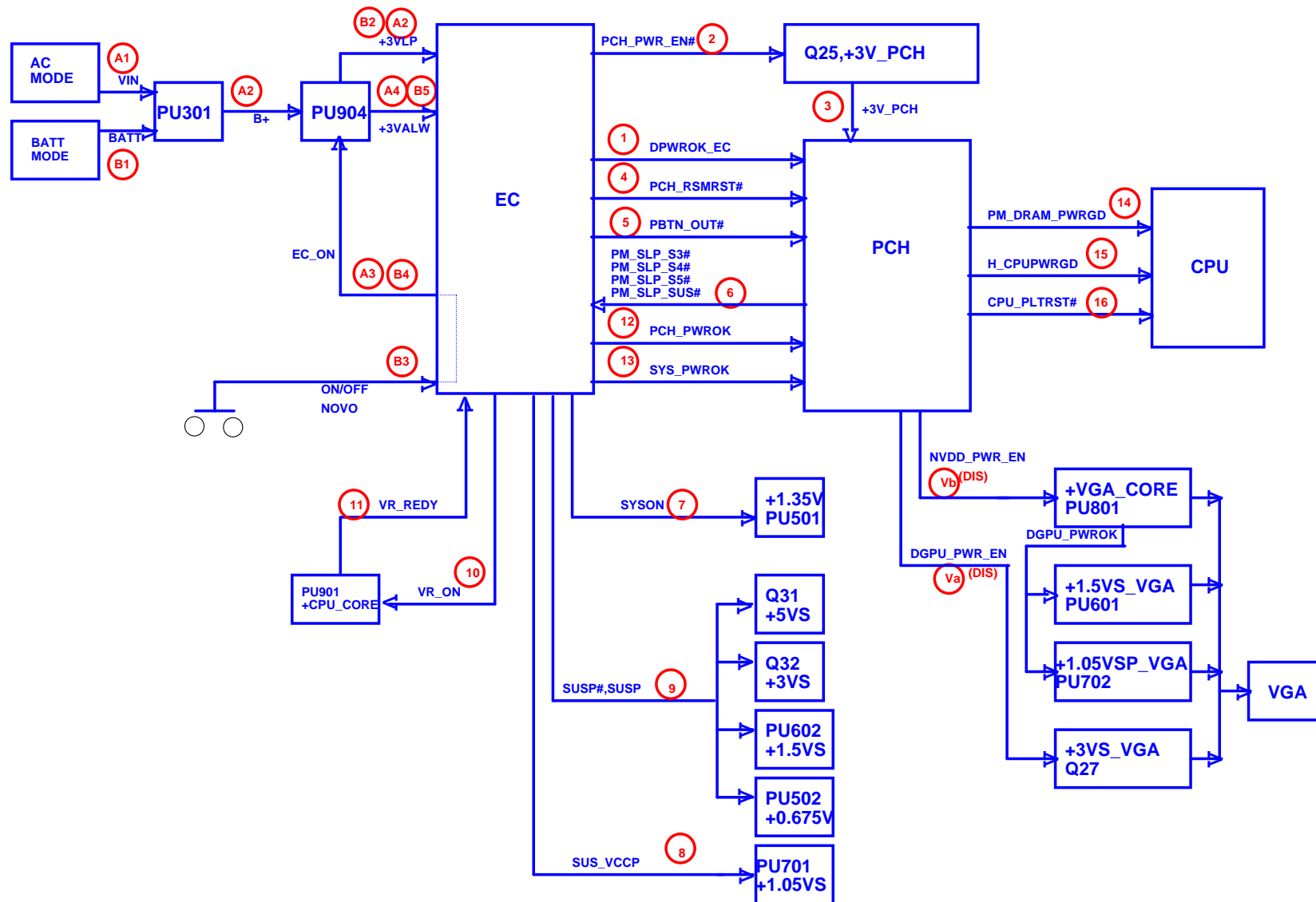
LED (For 15")



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Created	2012/12/14	2012/12/21		

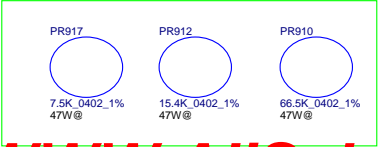
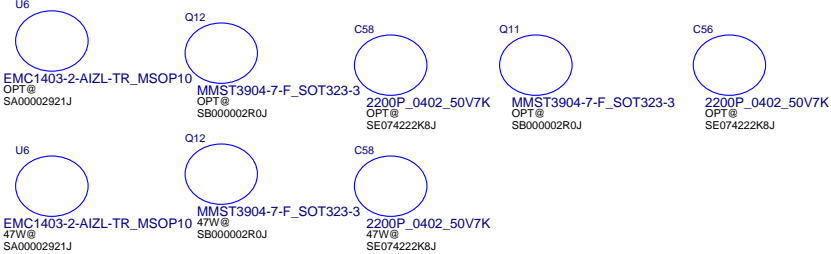
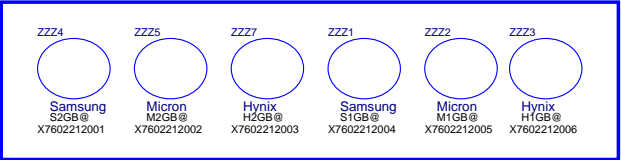
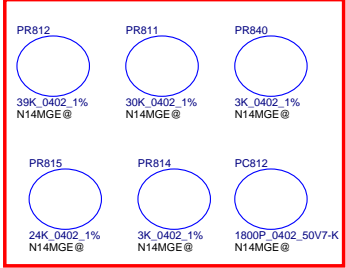
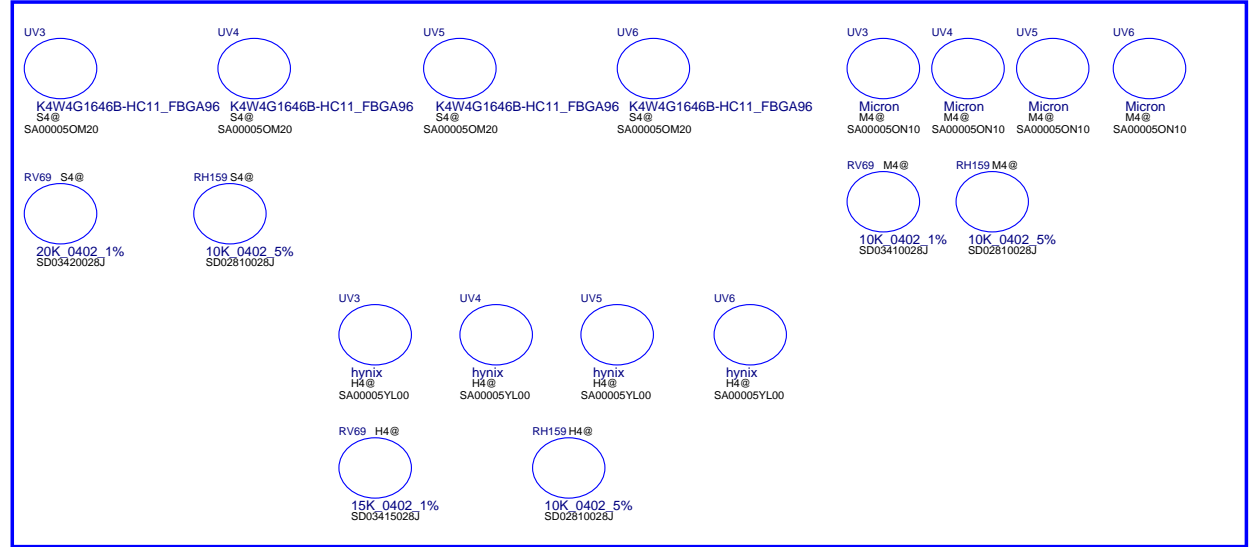
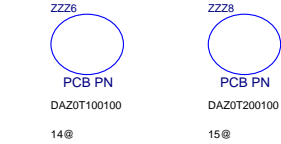
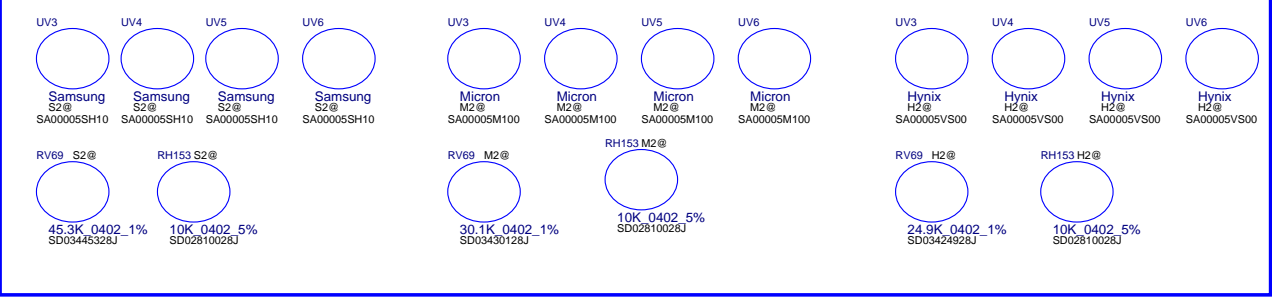
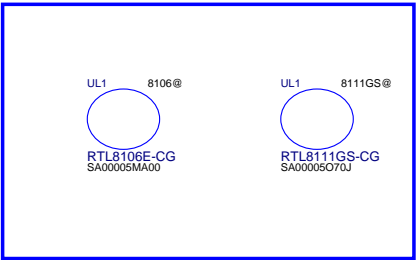


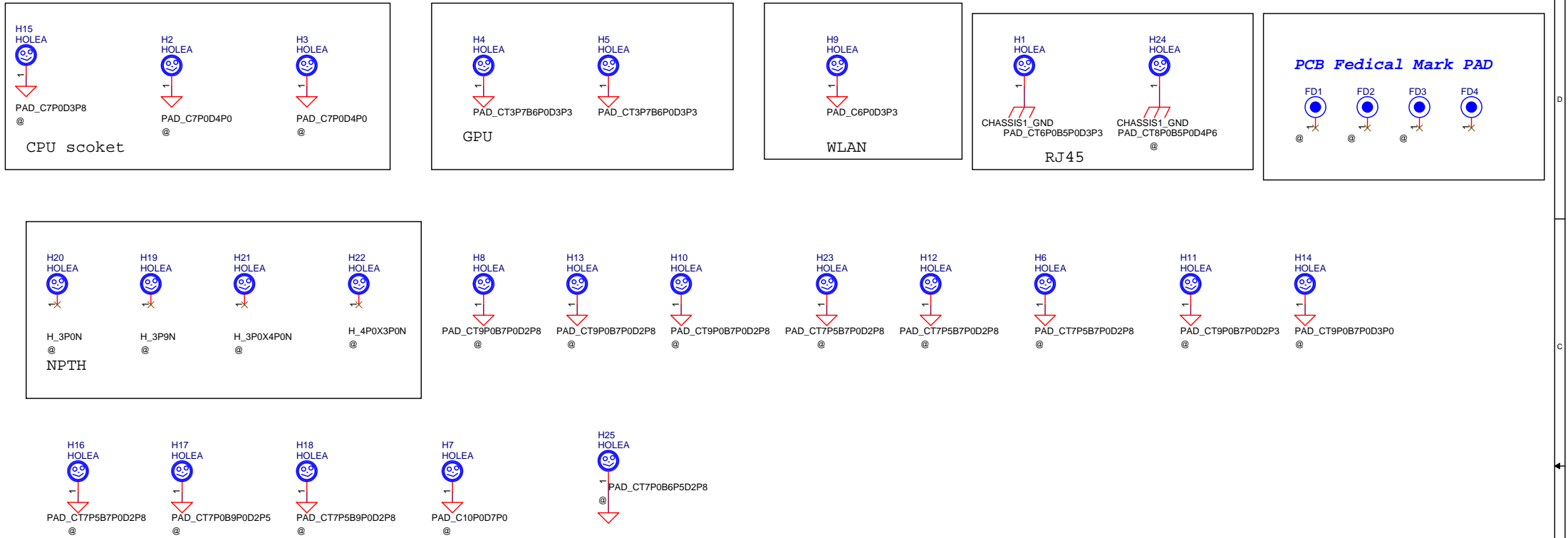
[illegible][illegible]



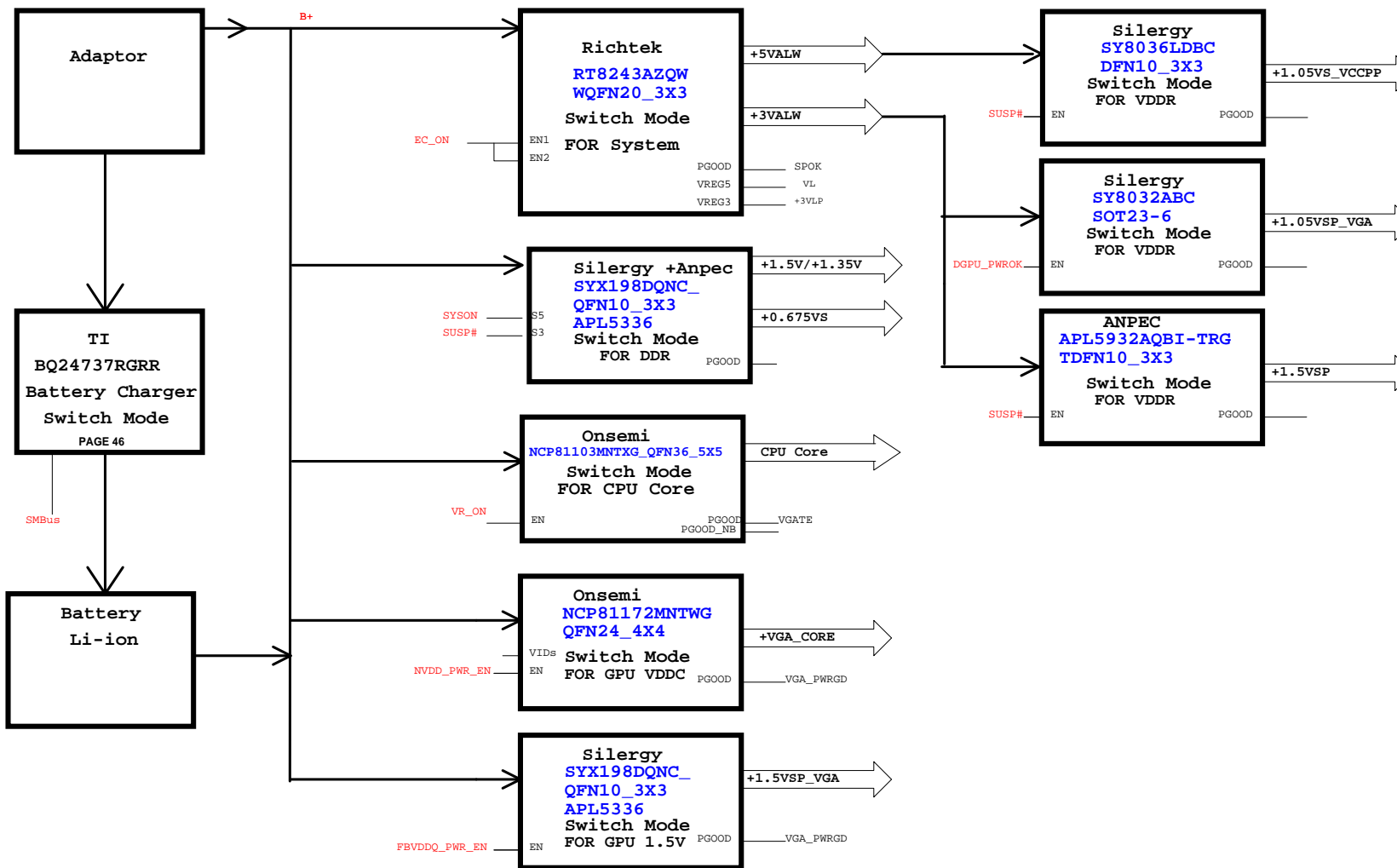
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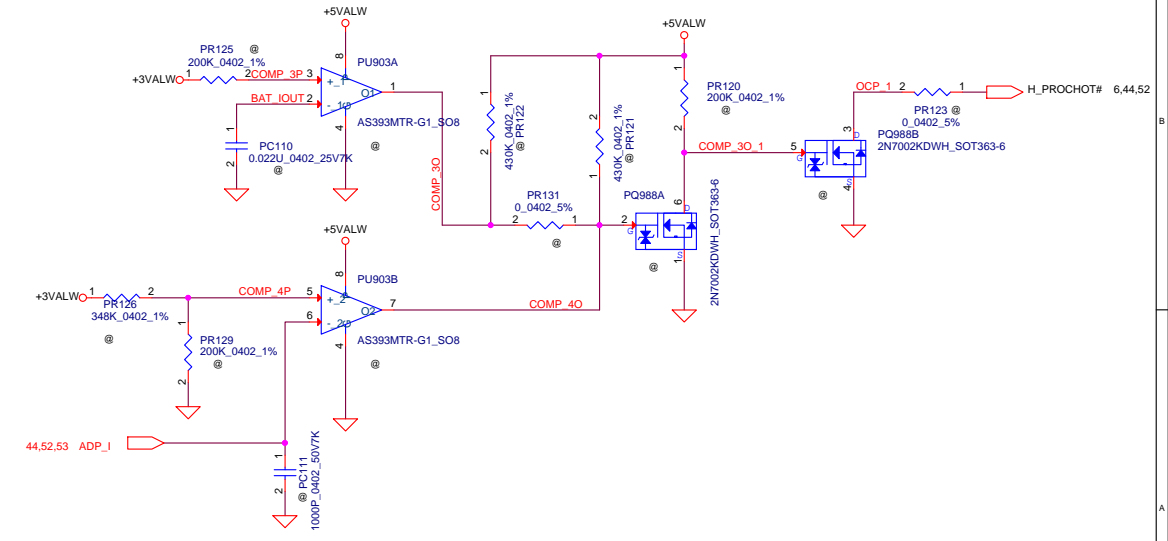
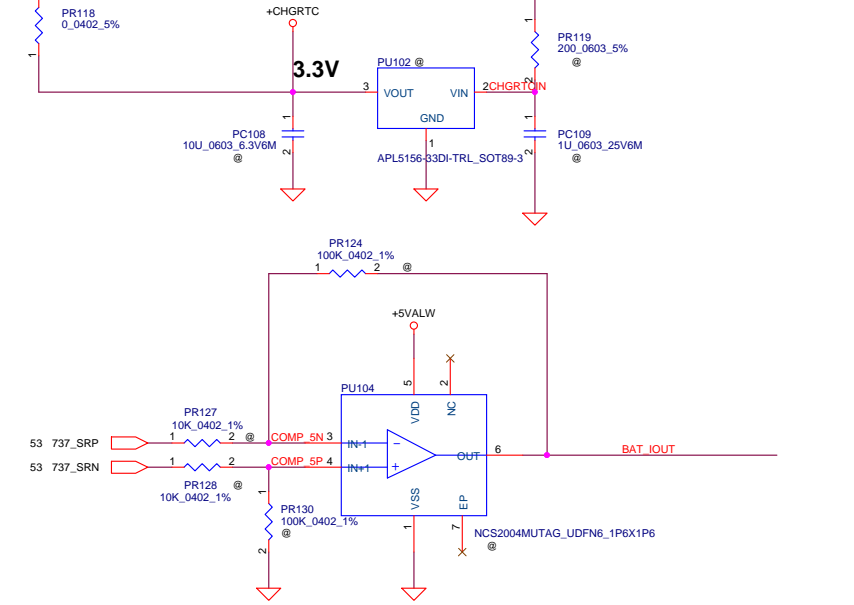
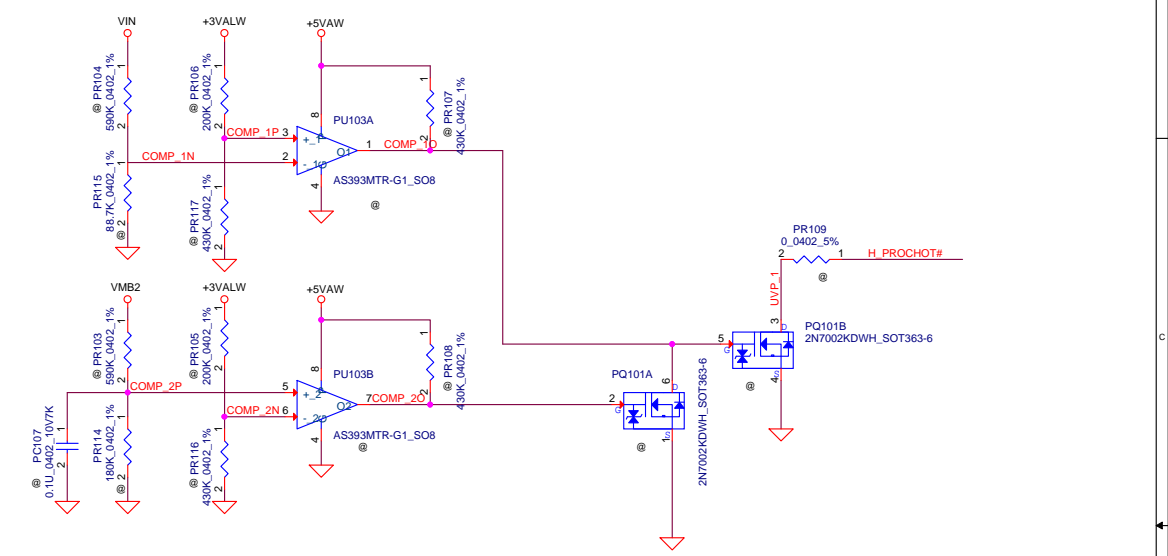
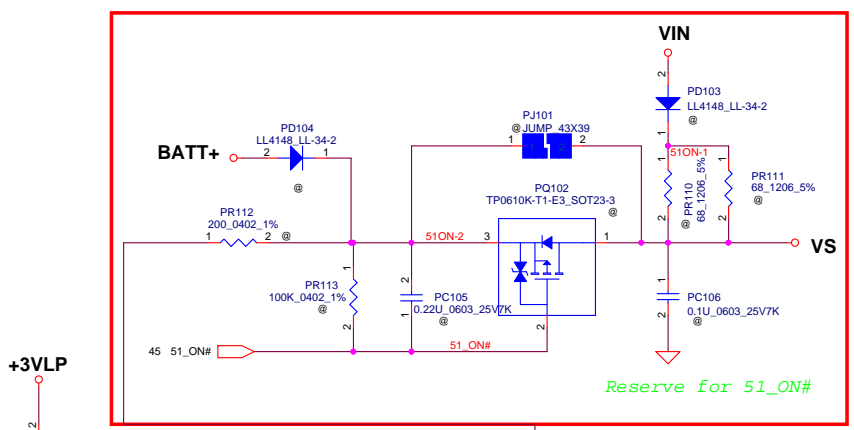
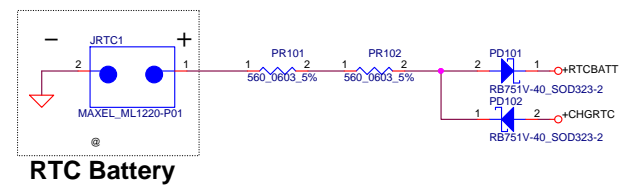
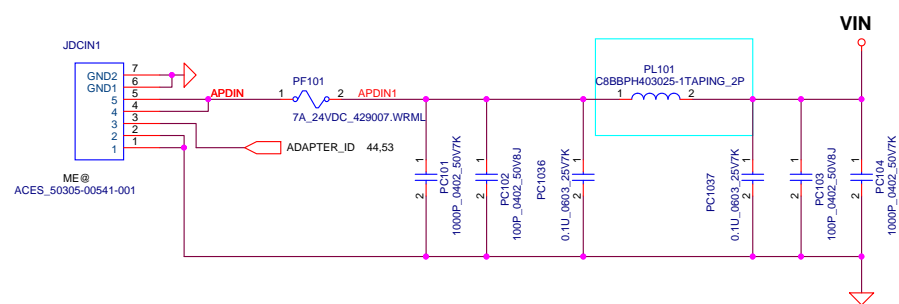
Title		LCFC	
Power sequence Block			
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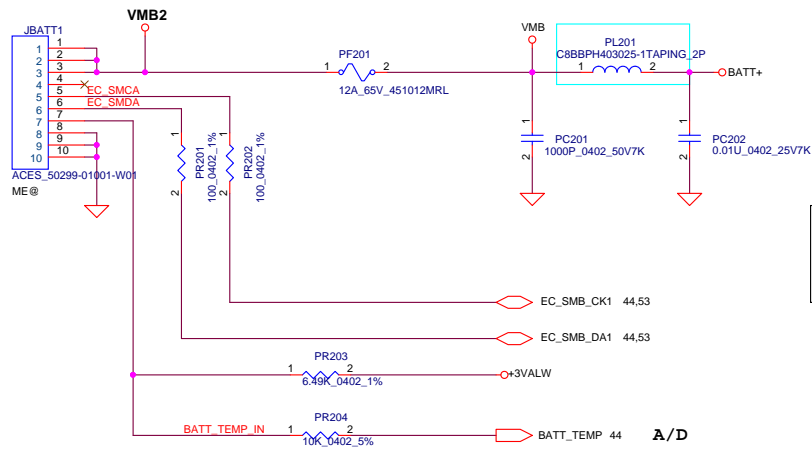
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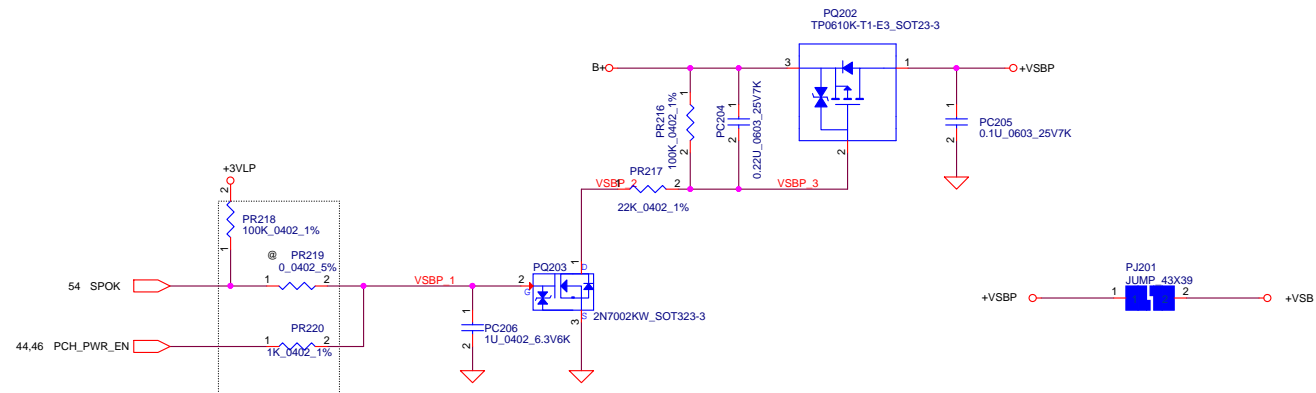
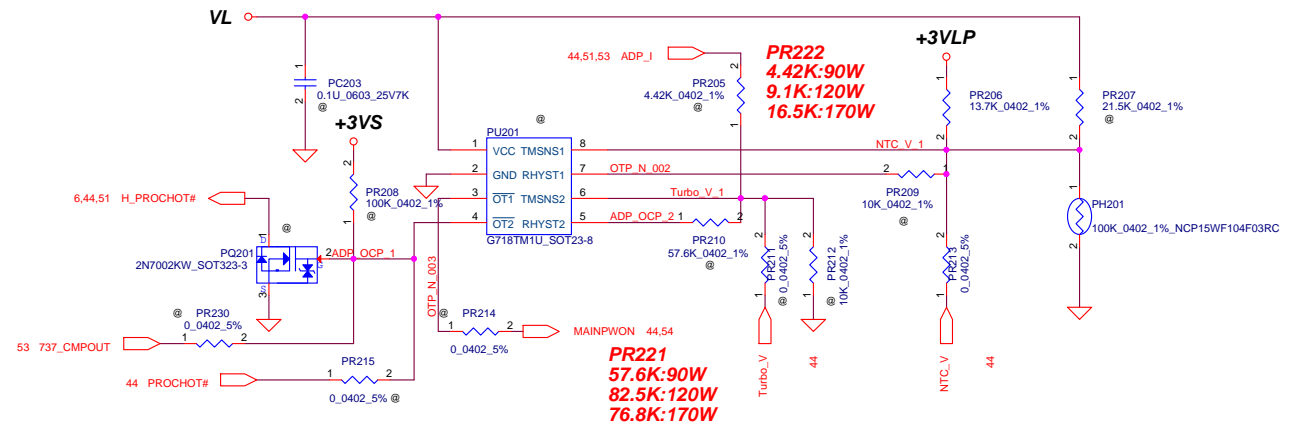
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<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>						DCIN / RTC charger					
						Size		Document Number		Rev	
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PH1 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



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44,46,56 SUSP#

44 SUS_VCCP

$$V_{FB} = 0.6V$$

$$V_O = V_{FB} * (1 + PR706 / PR705)$$


5A

Fsw=1MHZ
Vout=1.05V
OCP:7.5A

19,27,46,58 DGPU_PWROK

5A

Fsw=1MHZ
Vout=1.05V
OCP:7.5A

Security Classification		LC Future Center Secret Data		Title		
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				Size	Document Number	Rev
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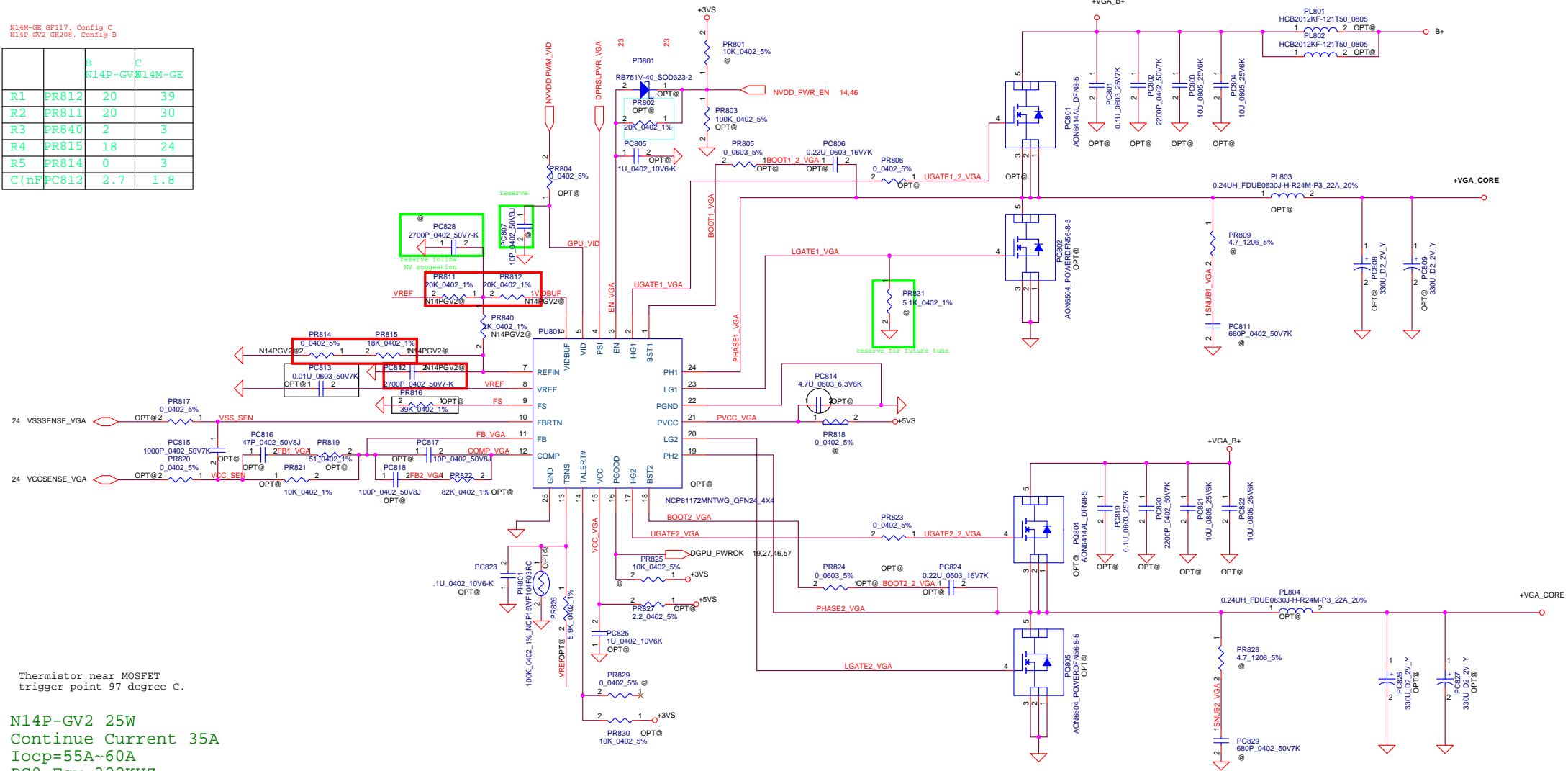
N14M-GE GP117, Config C
N14P-GV2 GK208, Config B

	B	C
R1	PR812 20	39
R2	PR811 20	30
R3	PR840 2	3
R4	PR815 18	24
R5	PR814 0	3
C(nF)	PC812 2.7	1.8

N14P-GV2 25W
Continue Current 35A
Iocp=55A~60A
PS0 Fsw=322KHZ
PS1/PS2 Fsw=475KHZ

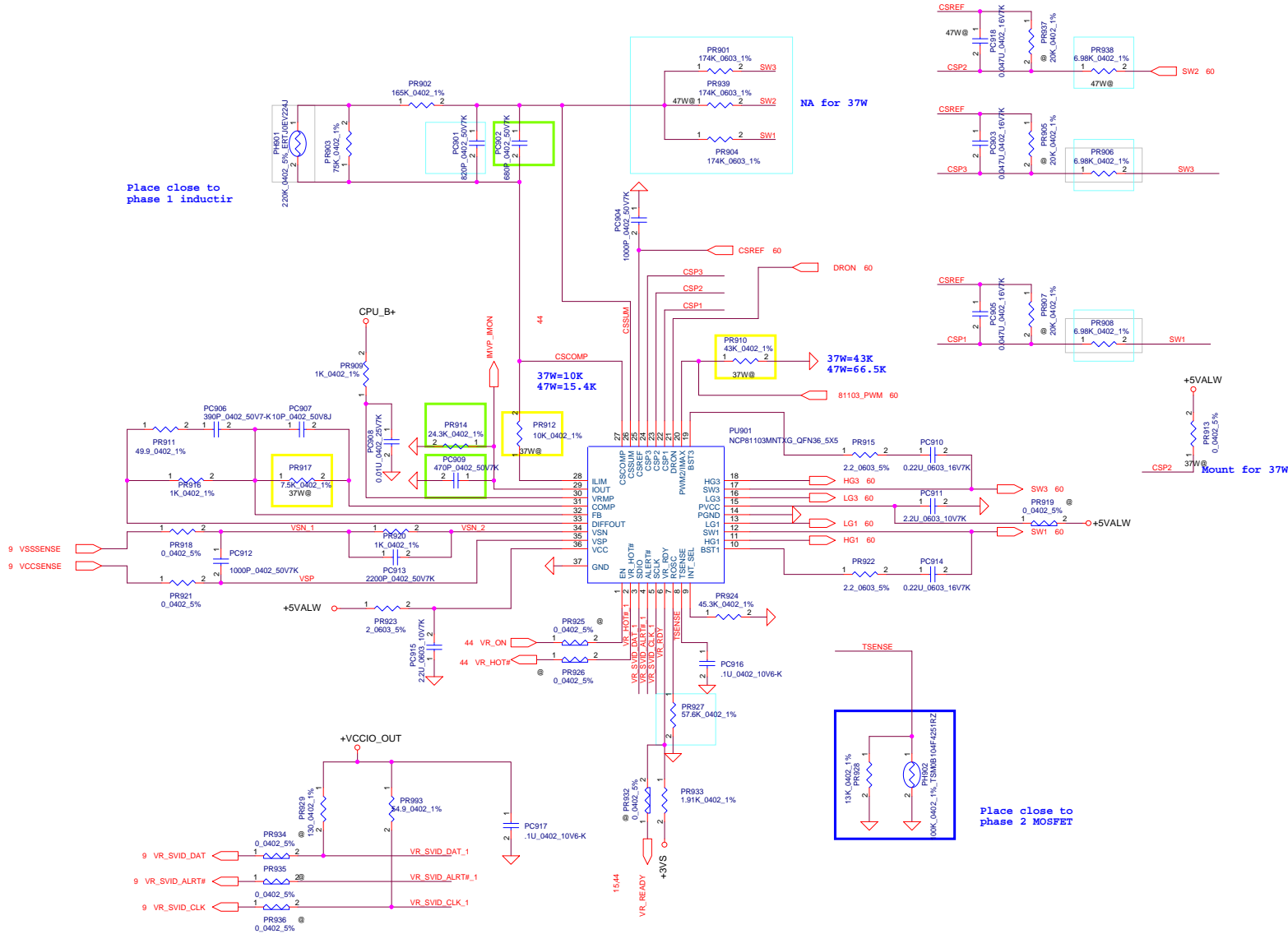
Vboot=0.9V

Thermistor near MOSFET
trigger point 97 degree C.



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				Size Custom	
				Document Number	
				401025	
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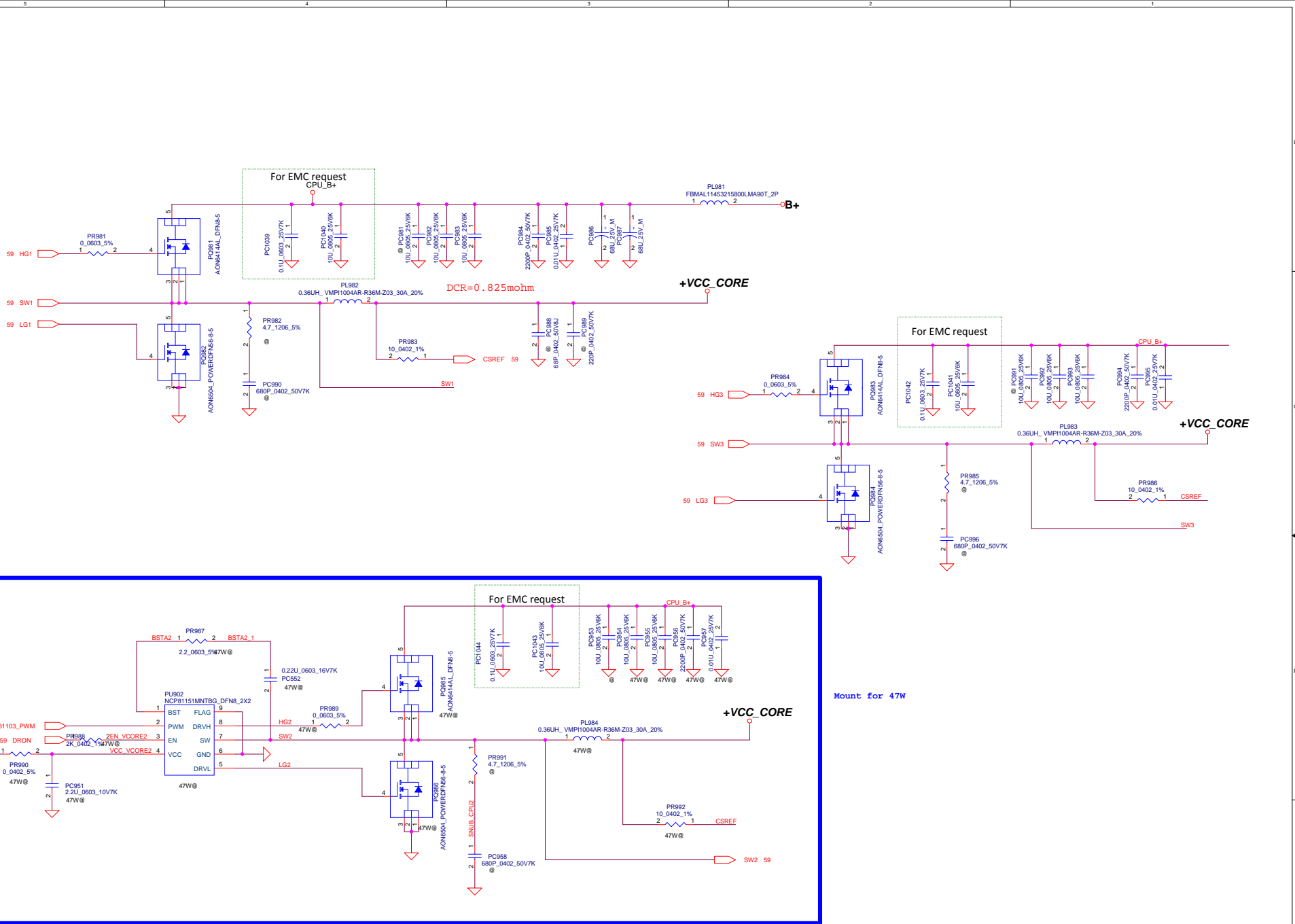
Place close to
phase 1 inductor



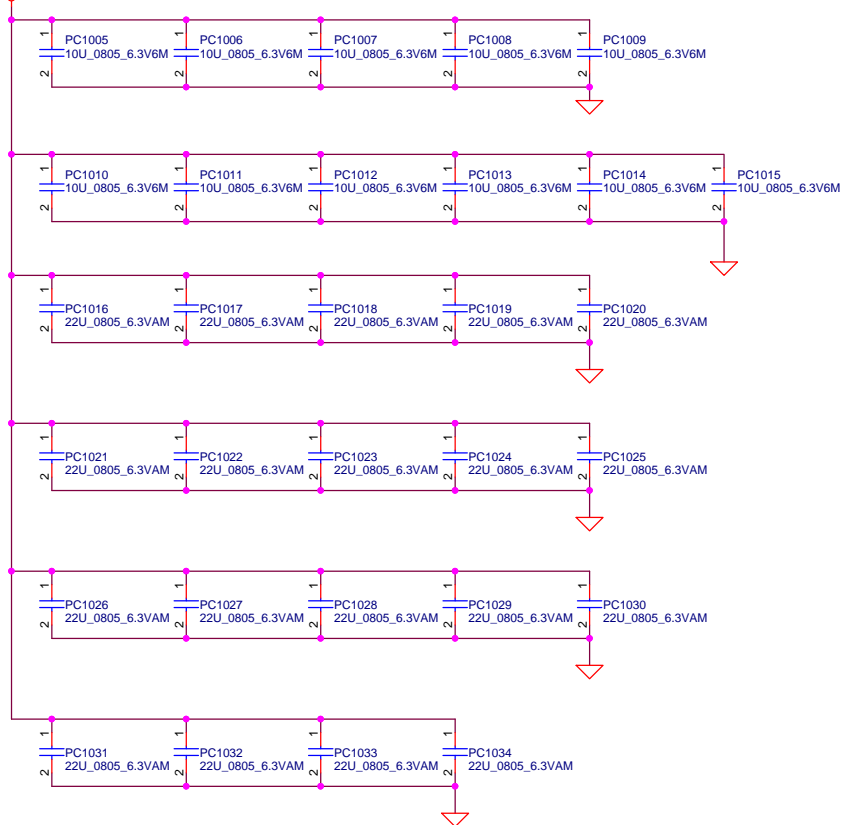
Place close to
phase 2 MOSFET

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				401025	
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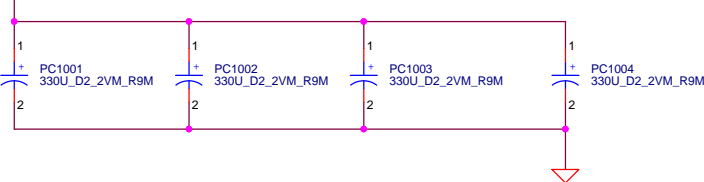




+VCC_CORE



+VCC_CORE



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